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(54) **COMPLEX-POLE LOAD OFFERING
CONCURRENT IMAGE REJECTION AND
CHANNEL SELECTION**

11/1213 (2013.01); *H04B 1/1036* (2013.01);
H04B 1/123 (2013.01); *H04L 27/3405*
(2013.01); *H04L 27/3809* (2013.01); *H04W*
4/008 (2013.01); *H03F 2200/294* (2013.01);
H03H 7/38 (2013.01); *H04B 2001/1072*
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CPC H04B 1/10; H04B 1/1638; H04B 1/1036;
H04B 15/00
USPC 375/316, 317, 319, 346, 350
See application file for complete search history.

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H01B 1/10 (2006.01)
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H04L 27/34 (2006.01)
H04L 27/38 (2006.01)
H03H 11/12 (2006.01)
H03F 3/193 (2006.01)

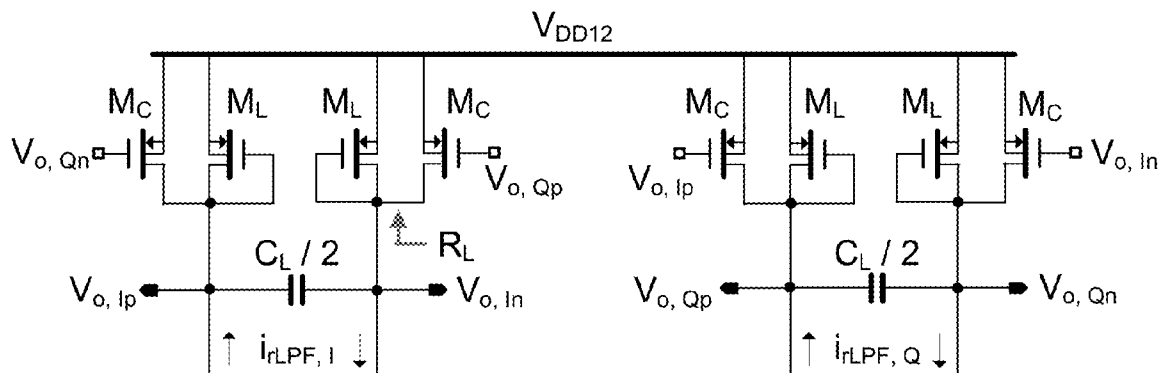
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Meyer; Jerald L. Meyer; Stanley N. Protigal

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(52) **U.S. Cl.**
CPC *H03H 11/04* (2013.01); *H03F 3/193*
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(57) **ABSTRACT**
A complex-pole load is configured as a parallel circuit,
having 4 transistors arranged in pairs. Each pair of transistors
has a transistor gated by a control voltage sources, and
connected in parallel with a transistor diode connected for
gating by the respective input. The control voltage sources
result in the circuit synthesizing a first order complex pole
at a positive IF (+IF) or a negative IF (-IF) for channel
selection and image rejection, offering image rejection and
channel selection concurrently.

2 Claims, 13 Drawing Sheets



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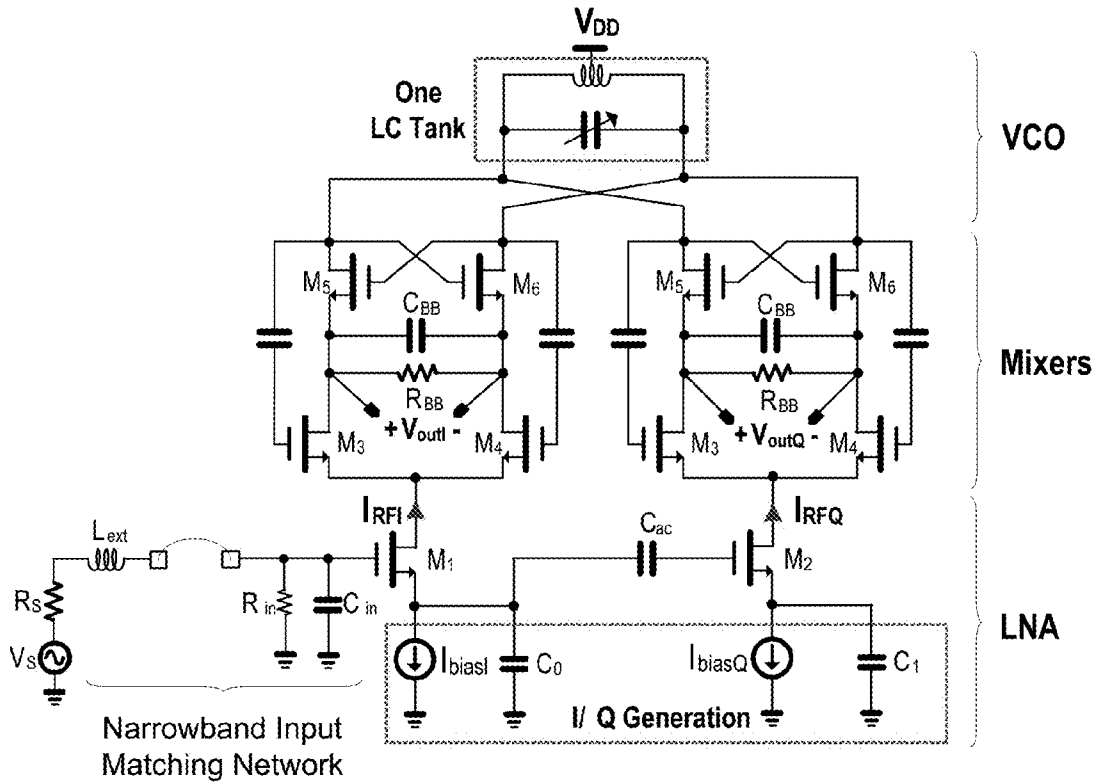


Fig. 1
(related art)

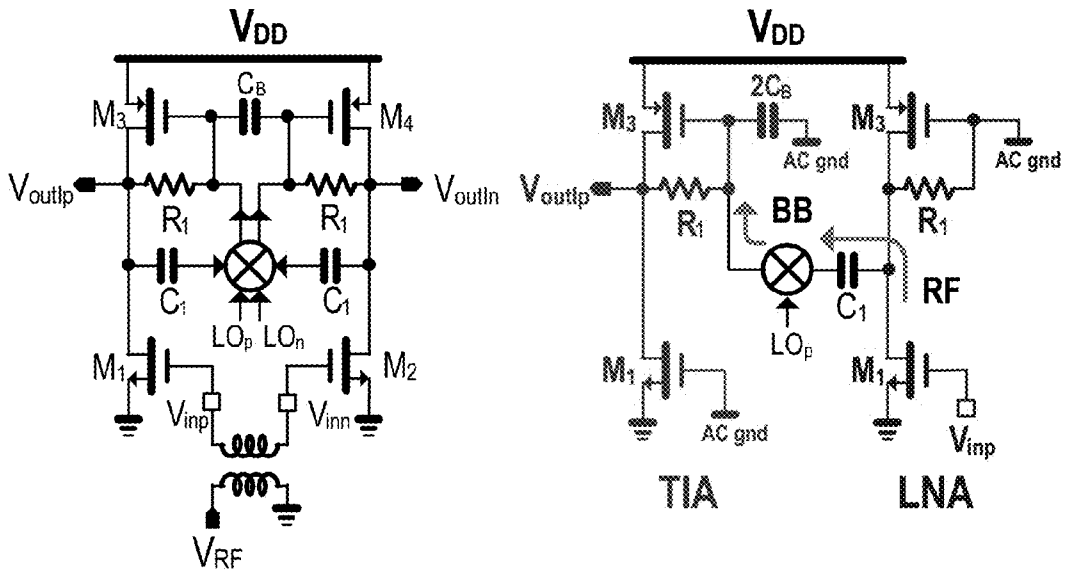


Fig. 2A
(related art)

Fig. 2B
(related art)

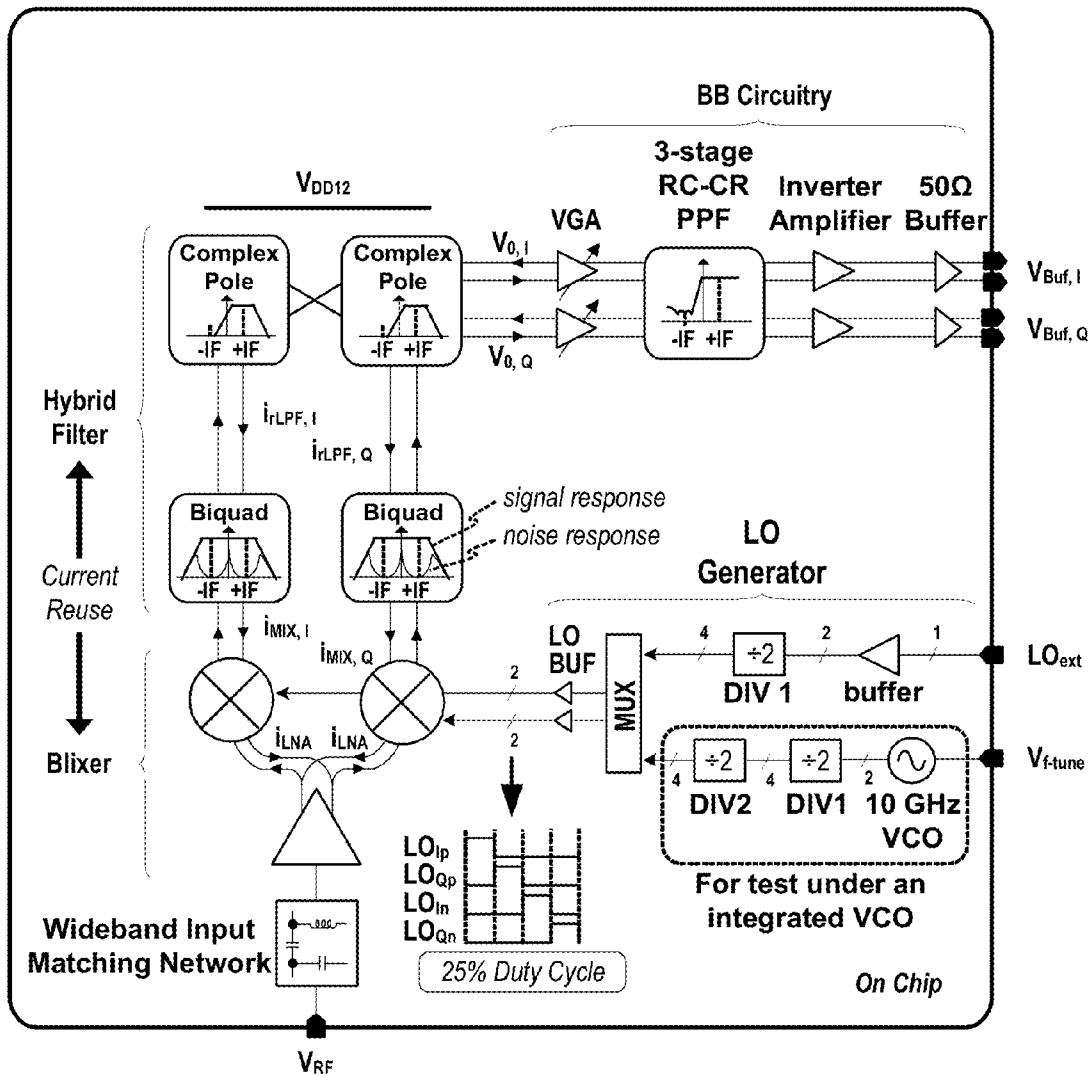


Fig. 3

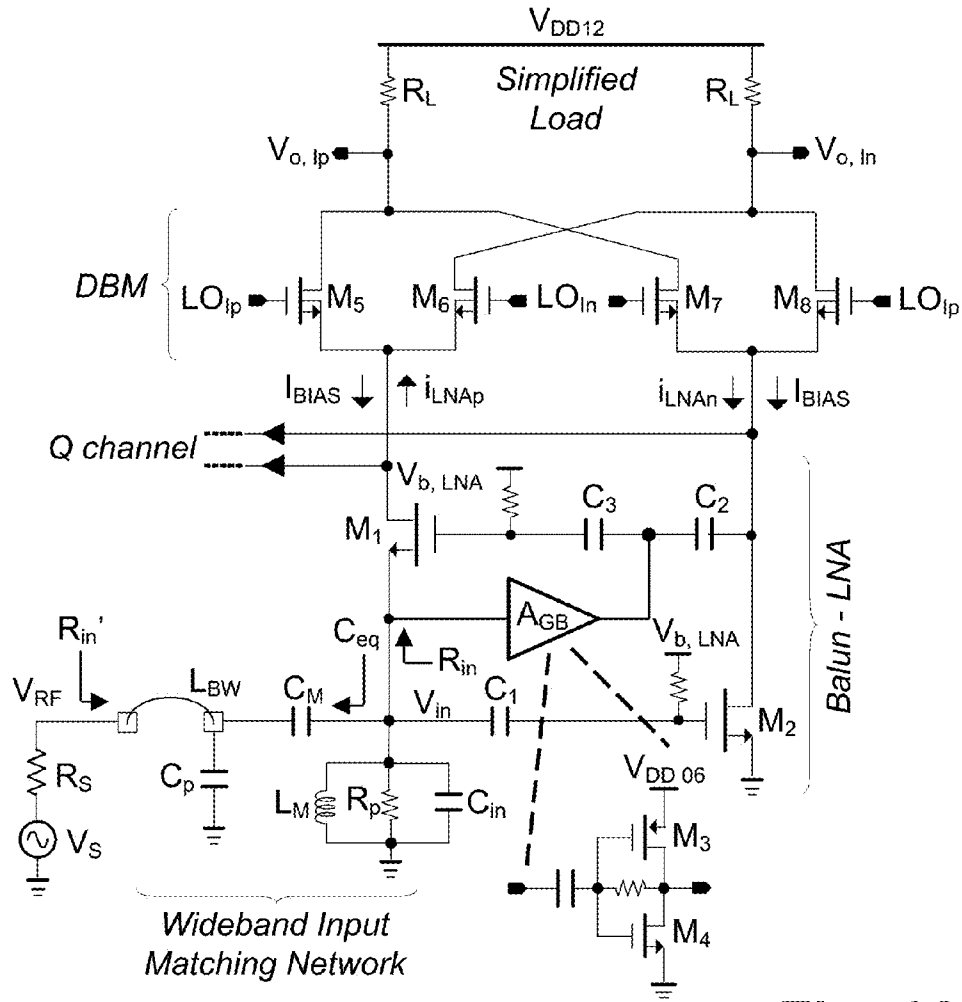


Fig. 4A

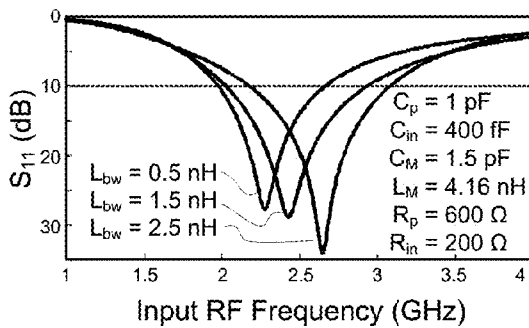


Fig. 4B

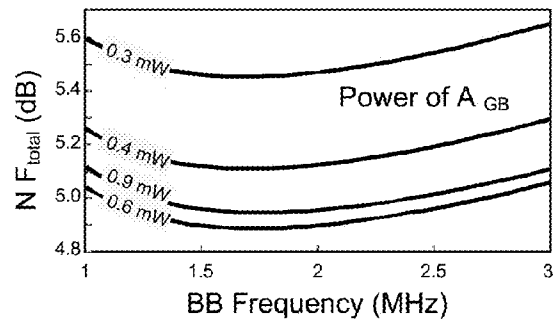


Fig. 4C

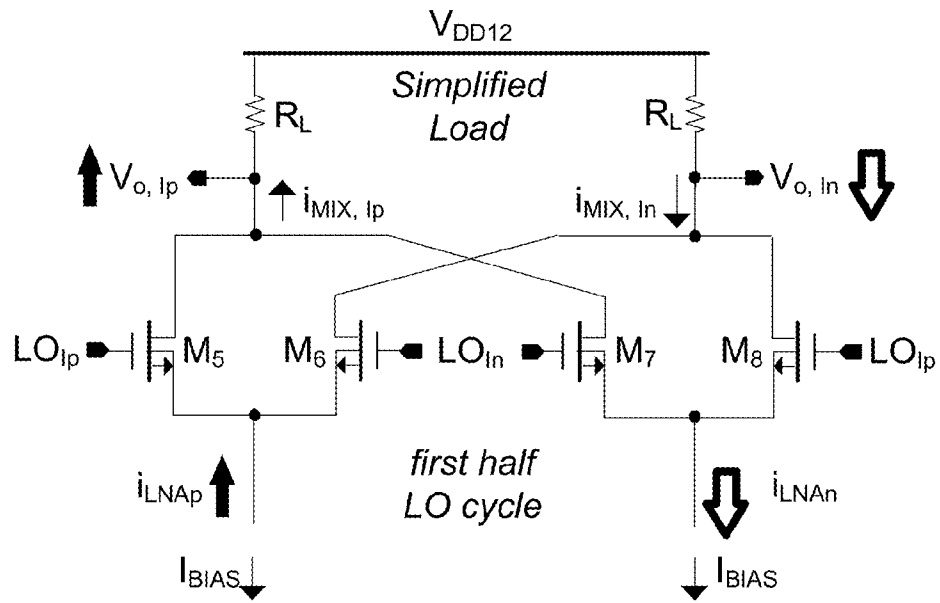


Fig. 5A

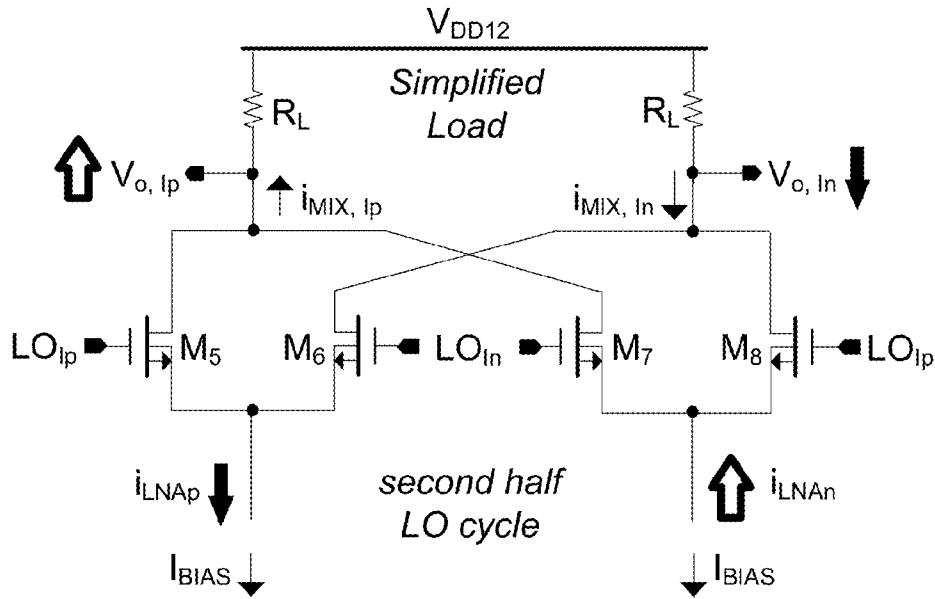


Fig. 5B

After One LO Cycle

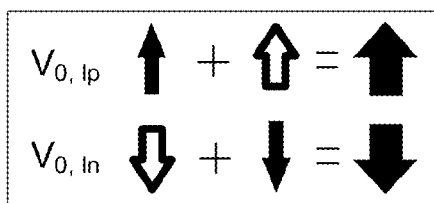


Fig. 5C

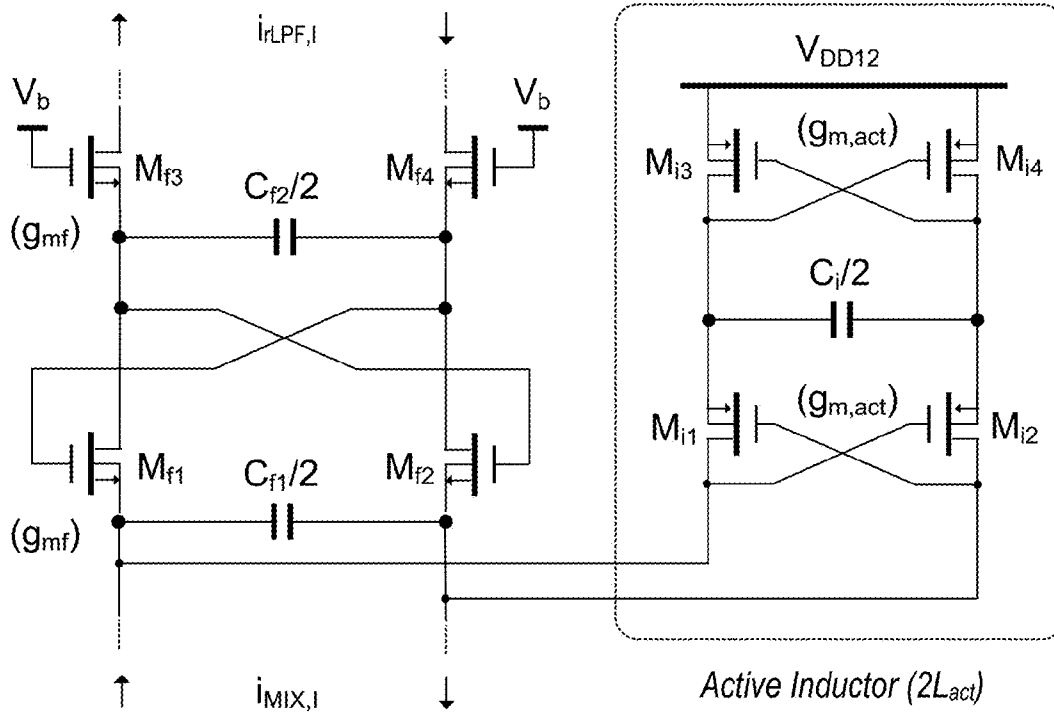


Fig. 6A

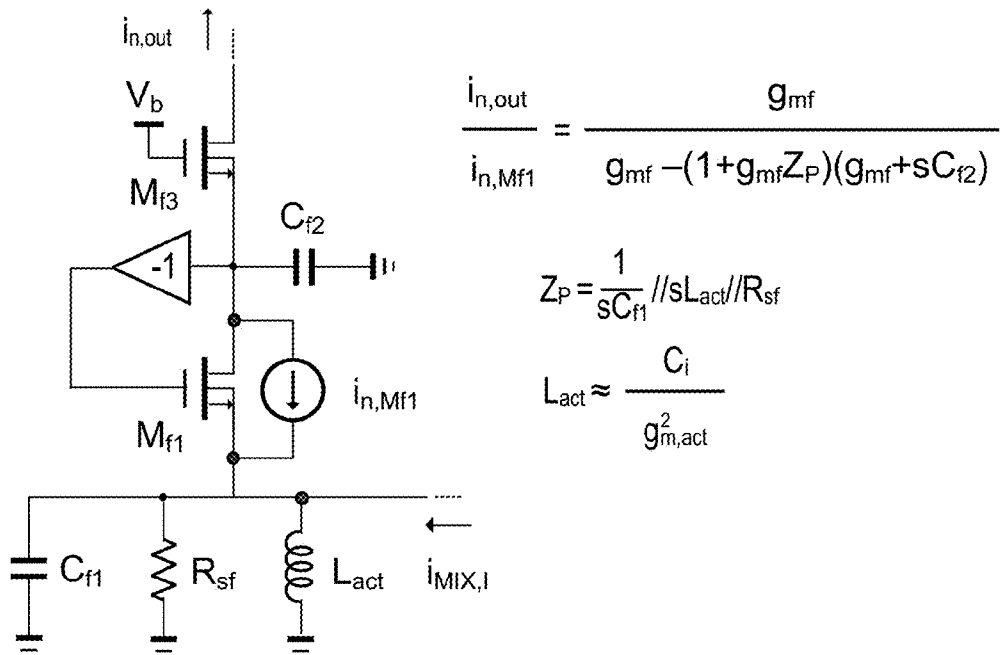


Fig. 6B

For $R_{sf} \gg sL_{act}$

A: $\omega \leq 0.1\omega_{or}$	\rightarrow	$Z_p \approx sL_{act}$
B: $0.1\omega_{or} < \omega < \omega_{or}$	\rightarrow	$Z_p \approx \frac{sL_{act}}{1 + s^2L_{act}C_{f1}}$
C: $\omega = \omega_{or}$	\rightarrow	$Z_p = R_{sf}$
D: $\omega_{or} < \omega < 10\omega_{or}$	\rightarrow	$Z_p \approx \frac{sL_{act}}{1 + s^2L_{act}C_{f1}}$
E: $\omega \geq 10\omega_{or}$	\rightarrow	$Z_p \approx \frac{1}{sC_{f1}}$

Fig. 7A

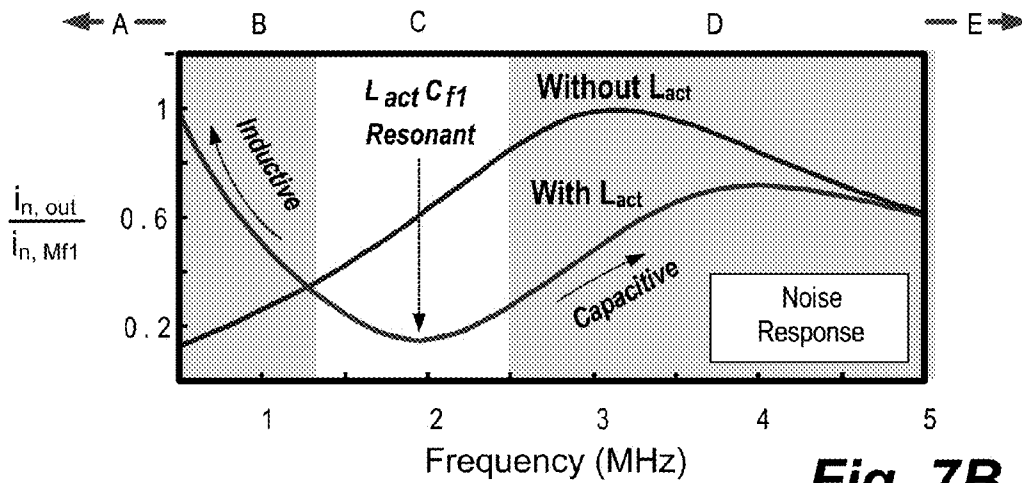


Fig. 7B

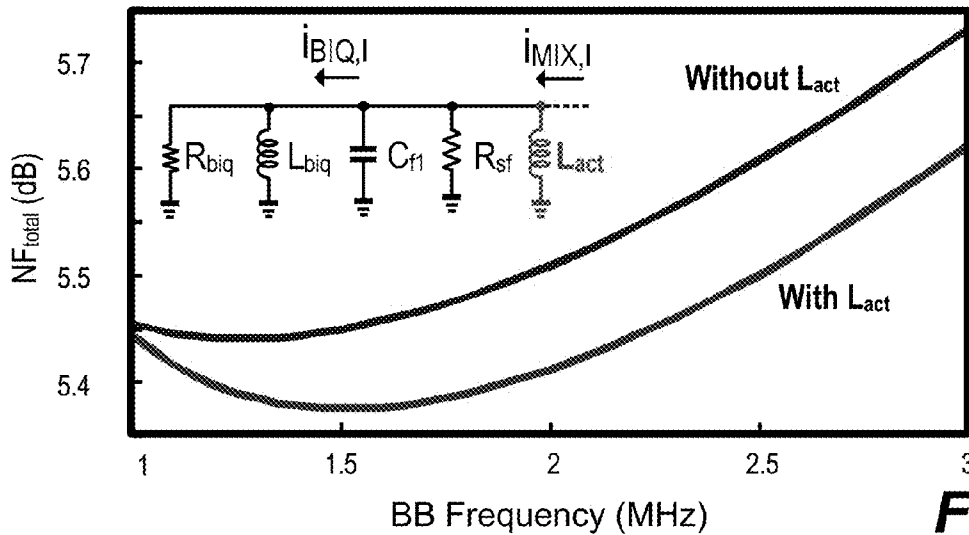


Fig. 8

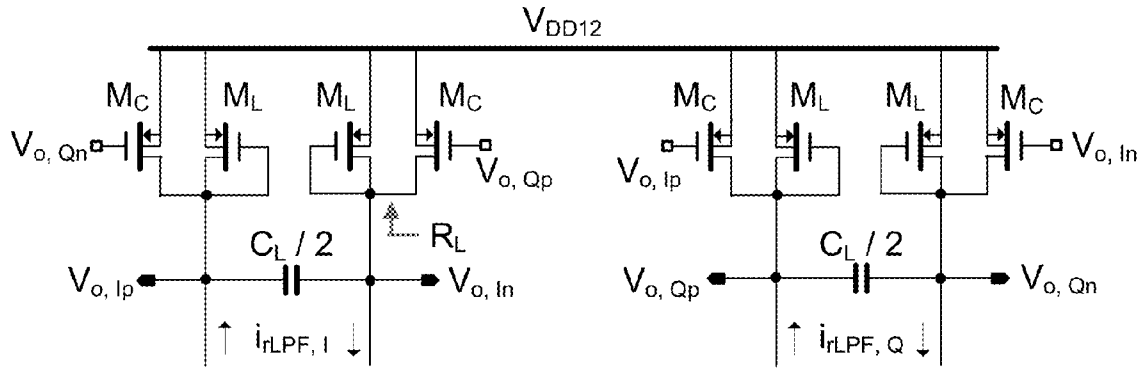


Fig. 9A

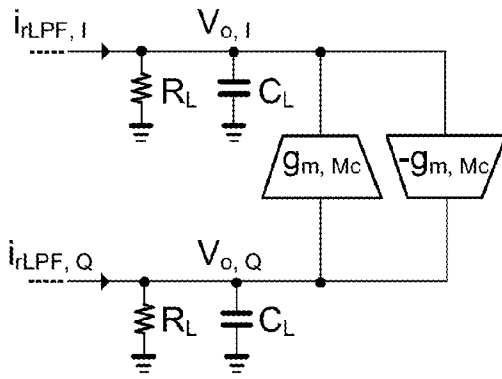
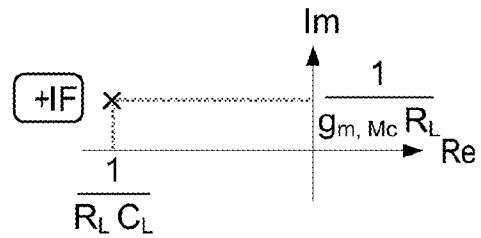


Fig. 9B



$$\frac{V_{o,I}}{i_{rLPF,I}} = \frac{R_L}{1 + sR_L C_L - jg_{m, Mc} R_L}$$

Complex - Pole Load

Fig. 9C

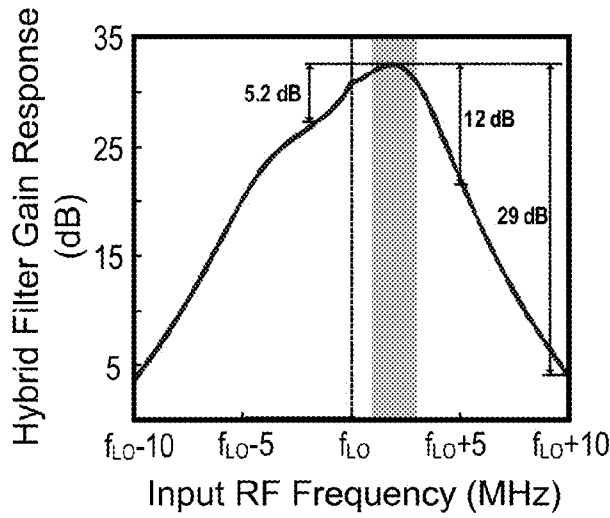


Fig. 10

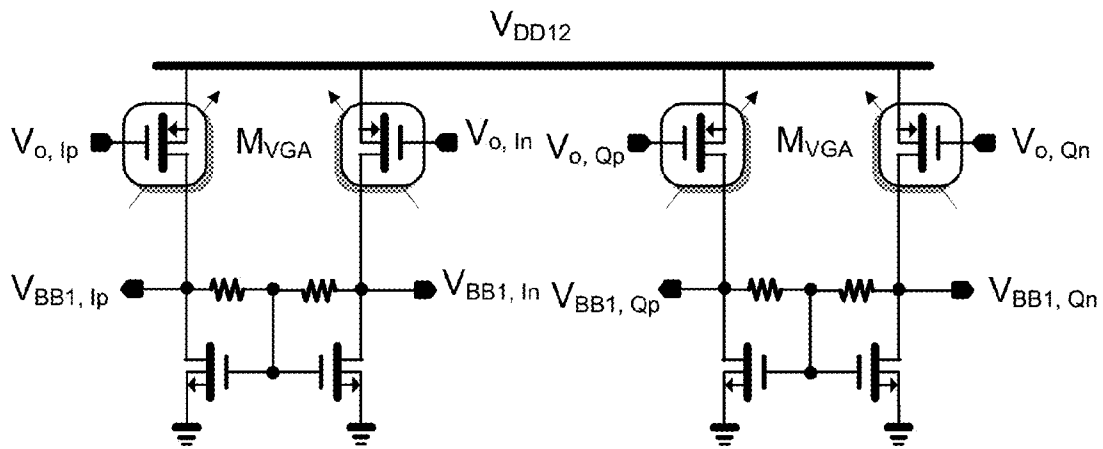


Fig. 11A

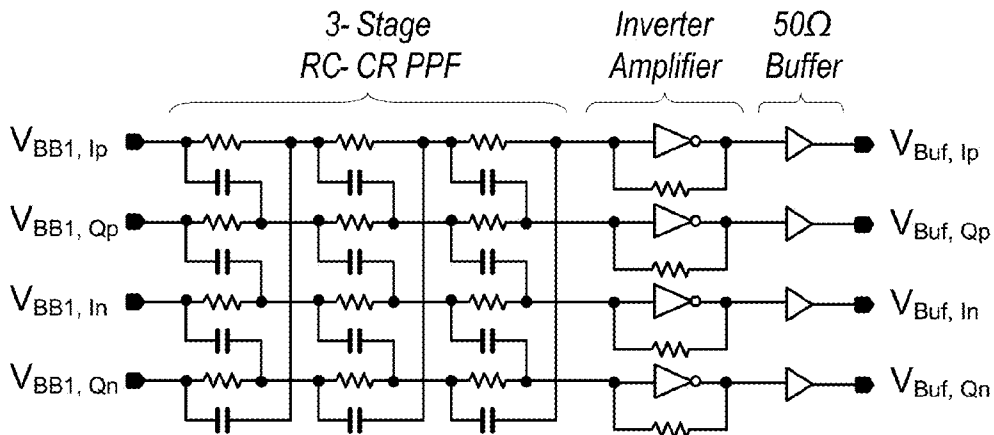


Fig. 11B

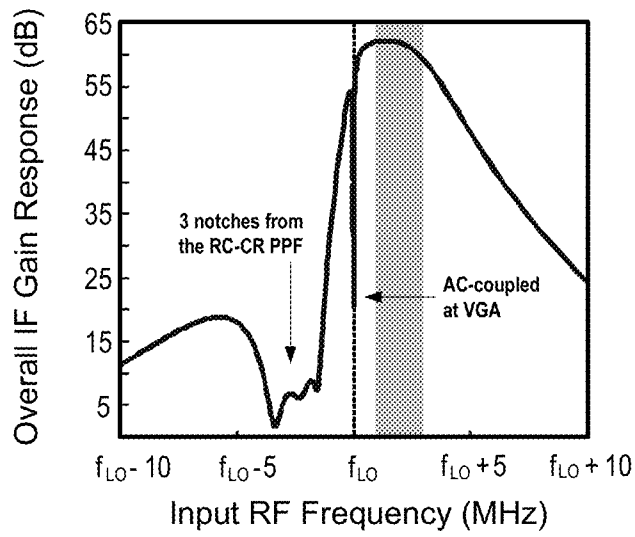


Fig. 12

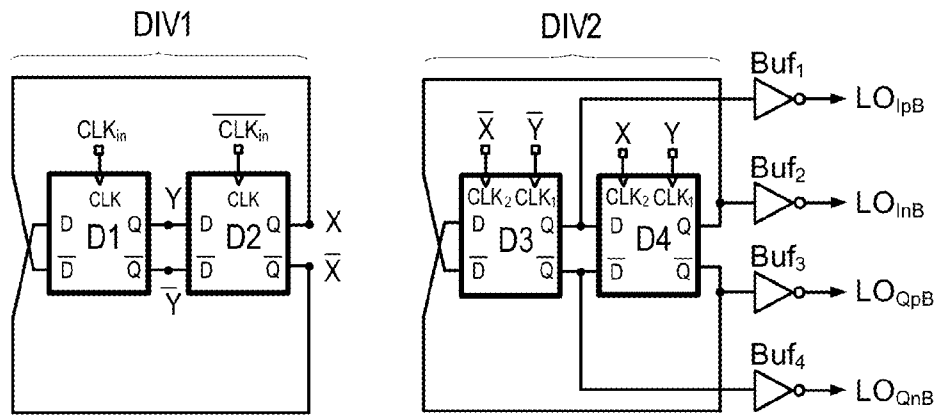


Fig. 13A

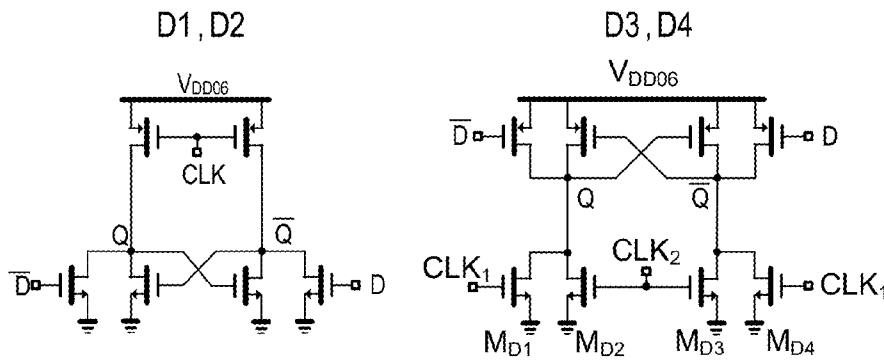


Fig. 13B

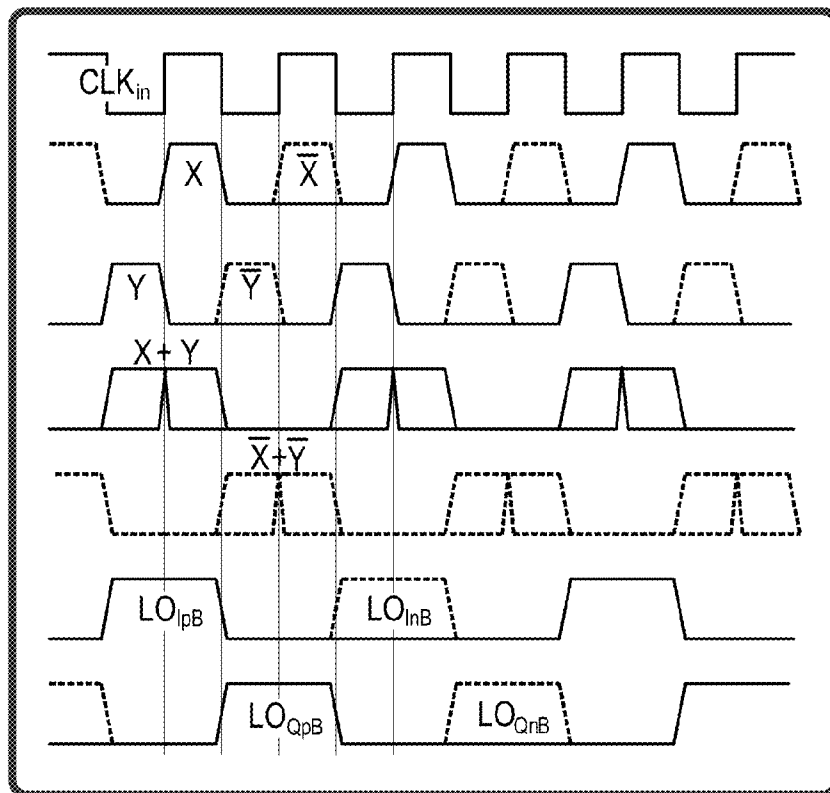


Fig. 13C

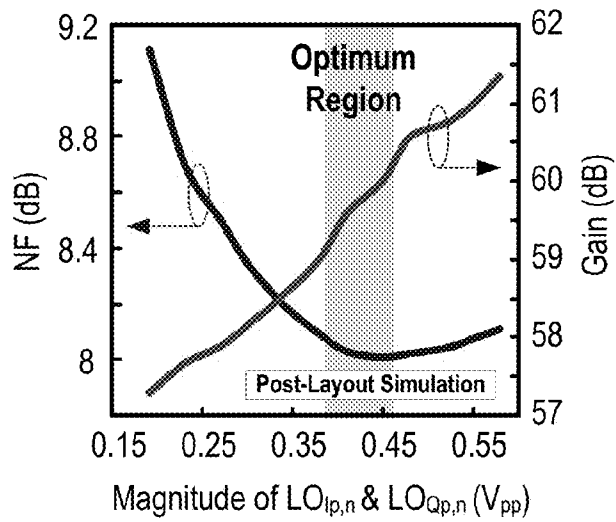


Fig. 14A

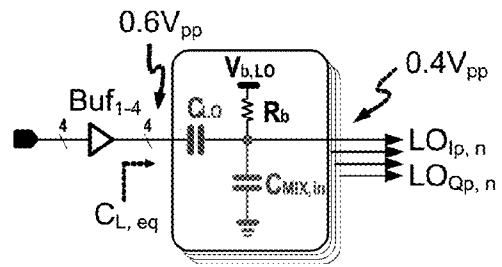


Fig. 14B

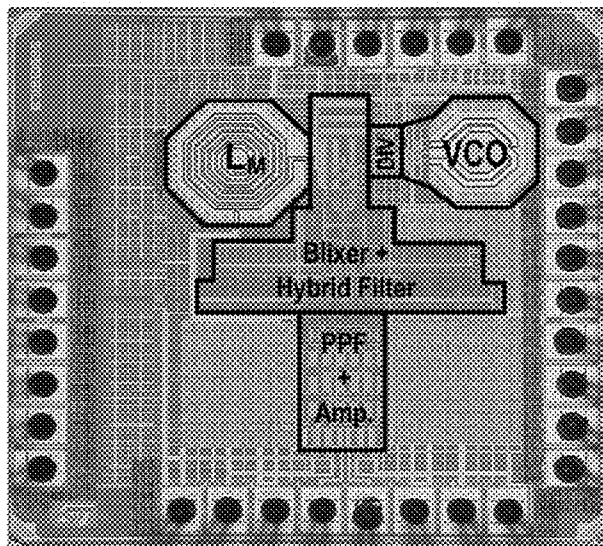


Fig. 15A

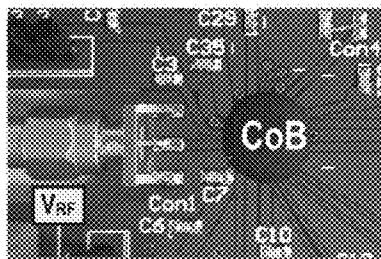


Fig. 15B

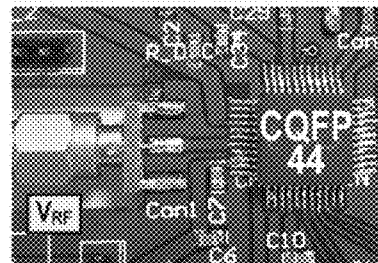


Fig. 15C

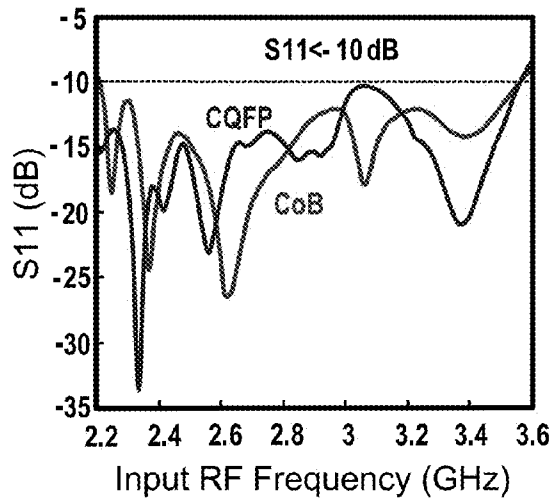


Fig. 16A

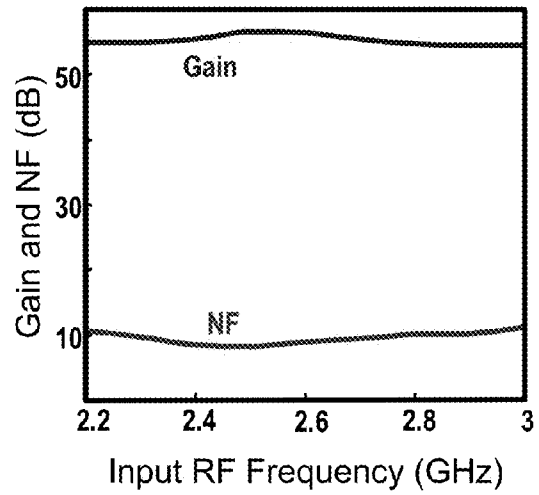


Fig. 16B

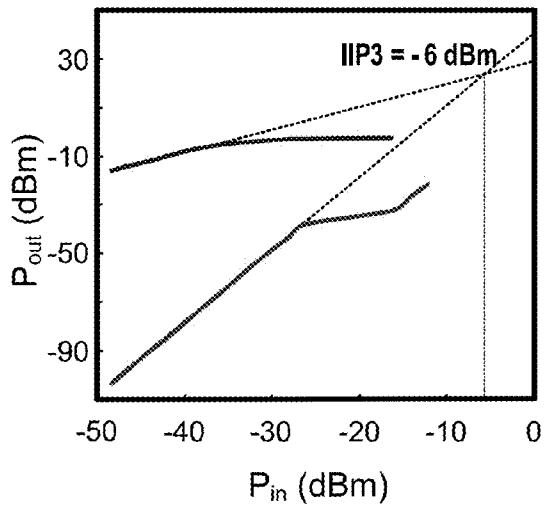


Fig. 16C

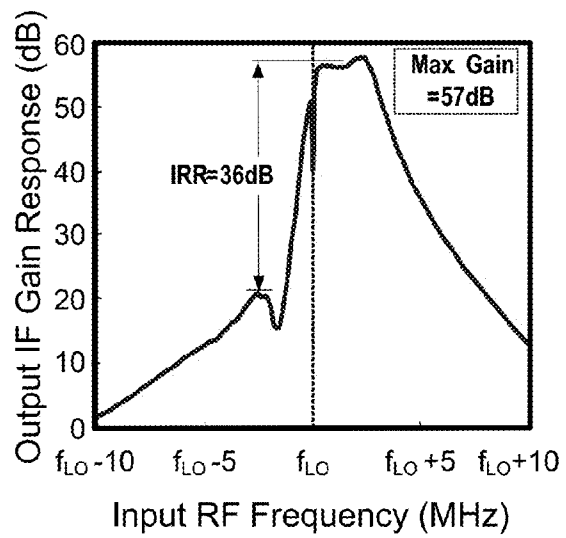


Fig. 16D

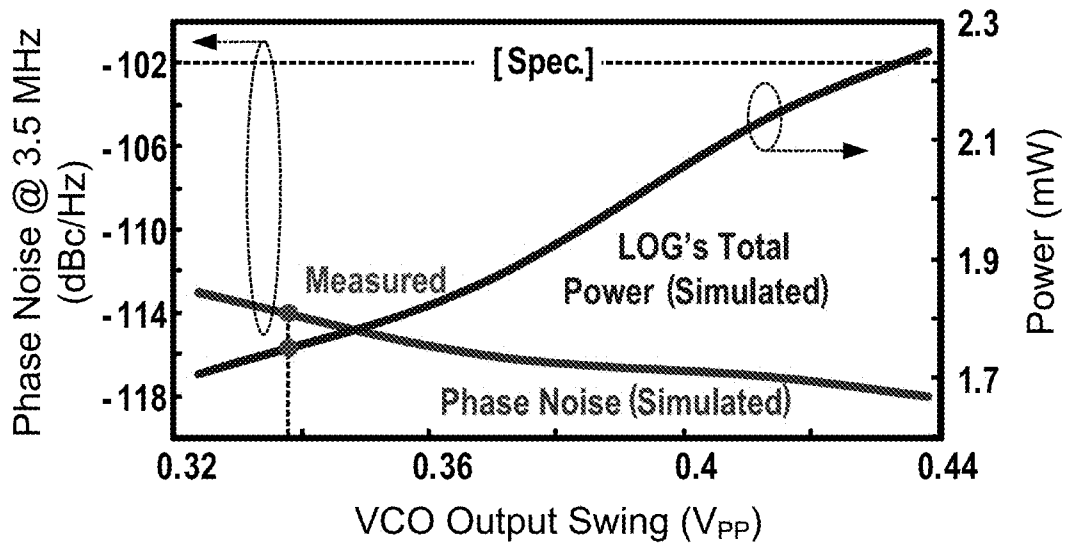


Fig. 17A

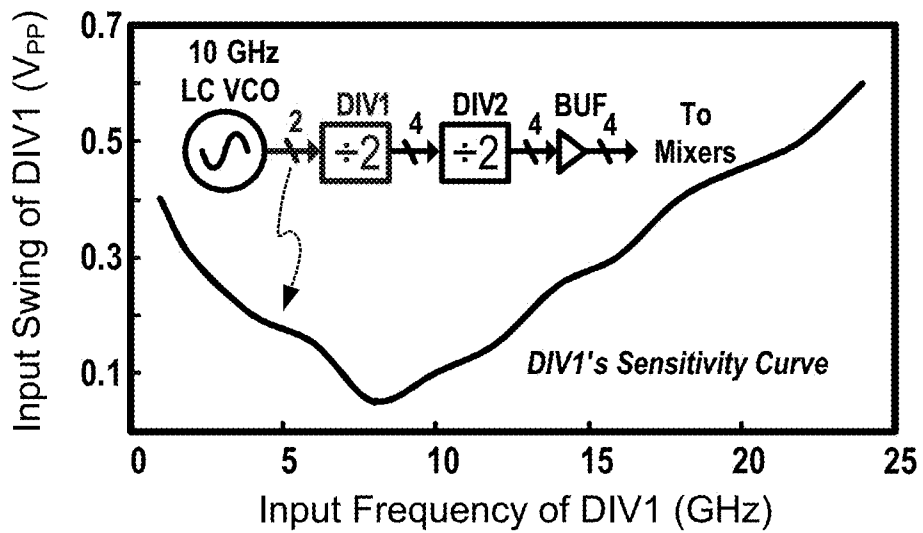


Fig. 17B

COMPLEX-POLE LOAD OFFERING CONCURRENT IMAGE REJECTION AND CHANNEL SELECTION

BACKGROUND

1. Field

The present disclosure relates to radio frequency (RF) signal interface circuits, and particularly to a complex-pole load used to provide channel selection and image rejection. Such complex pole loads are useful in baluns, mixers and filters.

2. Background

Ultra-low-power (ULP) radios have essentially underpinned the development of short-range wireless technologies such as personal/body area networks and Internet of Things. The main challenges faced by those ULP radios are the stringent power and area budgets, and the pressure of minimum external components to save cost and system volume. Balancing them with the performance metrics such as noise figure (NF), linearity and input matching involves many design tradeoffs at both architecture and circuit levels.

Ultra-low-voltage receivers have been extensively studied for short-range ZigBee, Bluetooth and energy-harvesting applications. Yet, the lack of voltage headroom will limit the signal swing and transistor's fT , imposing the need of bulky inductors or transformers to facilitate the biasing and tune out the parasitics. Thus, the die area is easily penalized, such as 5.76 mm^2 in and 2.5 mm^2 in one example. The current-reuse topologies should benefit more from technology scaling when the NF is less demanding. Advanced process nodes such as 65 nm CMOS feature sufficiently high- fT and low-VT transistors for GHz circuits to operate at very small bias currents. Unsurprisingly, when cascading the building blocks for current reuse, such as the low-noise amplifier (LNA) plus mixer, the RF bandwidth and linearity can be improved as well, by avoiding any high-impedance nodes at their interface.

Several NF relaxed current-reuse receivers have been reported. An example of an LNA mixer voltage controlled oscillator (VCO) (LMV) cell is illustrated in FIG. 1. In this example, the mixer uses an external LMV cell L_{ext} for narrowband input matching and pre-gain. One LC-tank VCO saves the chip area, but putting the I/Q generation in the LNA (M_1 - M_2) degrades the NF. Only single-balanced mixers (M_3 - M_4) can be used.

Sharing the bias current among more blocks saves power (2.4 mW), but the NF, gain and the input port voltage reflection coefficient (S_{11}) are sensitive to its external high-Q inductor (L_{ext}) for narrowband input matching and passive pre-gain. Also, under the same bias current, it is hard to optimize the LNA's NF (RF path) with the phase noise of the VCO (LO path). Finally, although a single VCO can save area, the I/Q generation has to be embedded into the LNA. This structure leads to a 3 dB gain loss deteriorating the NF (12 dB), while rendering the I/Q accuracy more susceptible to process variations.

To return the I/Q generation back to the LO path, one GPS receiver design adopts two VCOs to tailor a quadrature LMV (QLMV) cell. Although its power is further optimized (1 mW), three on-chip inductors and one off-chip balun are entailed, penalizing die size and system costs. Also, both LMV and QLMV cells share the same pitfall that only a 50% duty cycle LO (50% LO) can be used for the mixing, which is less effective than 25% LO in terms of gain (i.e., 3 dB higher), NF and I/Q isolation. Finally, as their baseband (BB) channel selection and image rejection are out of their

current-reuse paths, any large out-band blockers are necessarily converted into voltages before filtering. This fact constitutes a hard tradeoff between noise, linearity and power (i.e., 1.2 mW baseband power in one example and 5.2 mW baseband power in the above-mentioned GPS receiver).

Another example is a current-reuse circuit-reuse receiver, which merges the RF LNA and baseband transimpedance amplifier (TIA) in one cell, shown in FIG. 2A, in which a circuit-reuse receiver merges an RF LNA and BB TIA. A conceptual view of its operation is given in FIG. 2B, which shows a single-ended equivalent circuit of FIG. 2A, illustrating its RF-to-BB operation conceptually (from right to left).

Without the VCO, and by using passive mixers, this topology can reserve more voltage headroom for the dynamic range. An RF balun is nevertheless entailed for its fully-differential operation, and several constraints limit its NF and linearity: 1) the LNA and TIA must be biased at the same current; 2) the LNA's NF should benefit more from short-channel devices for $M1$ - 2 , but the baseband TIA prefers long-channel ones to lower the $1/f$ noise; and 3) any out-band blockers will be amplified at the LNA's (TIA's) output before deep baseband filtering.

SUMMARY

A complex-pole load is configured as a parallel circuit, comprising 4 transistors arranged in pairs. Each pair of transistors comprises a transistor gated by a control voltage sources, and connected in parallel with a transistor diode connected for gating by the respective input. The control voltage sources result in the circuit synthesizing a first order complex pole at a positive IF (+IF) or a negative IF (-IF) for channel selection and image rejection, offering image rejection and channel selection concurrently.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic circuit diagram showing LMV cell. L_{ext} is external for narrowband input matching and pre-gain. One LC tank VCO saves the chip area, but putting the I/Q generation in the LNA (M_1 - M_2) degrades the noise figure (NF). Only single-balanced mixers (M_3 - M_4) can be used.

FIGS. 2A and 2B are schematic circuit diagrams showing circuit configurations. FIG. 2A is a schematic circuit diagram showing a circuit-reuse receiver merging RF LNA and baseband TIA. FIG. 2B is a schematic circuit diagram showing a single-ended equivalent circuit illustrating its RF-to-BB operation conceptually (from right to left).

FIG. 3 is a schematic circuit diagram showing an RF-to-BB current-reuse ZigBee receiver.

FIGS. 4A-C are diagrams showing a wideband input matching network, balun LNA and I/Q DBMs. FIG. 4A is a schematic circuit diagram showing the wideband input matching network, balun LNA and I/Q double balanced mixers (Q channel is omitted and the load is simplified as R_L). FIG. 4B is a graph showing a variation of the input port voltage reflection coefficient (S_{11}) bandwidth with bondwire inductance L_{BW} . FIG. 4C is a graph showing a Power of A_{GB} versus NF.

FIGS. 5A and 5B are a schematic circuit diagram showing operation of the I-channel double balanced mixer. It inherently offers output balancing after averaging in one LO cycle as shown in their FIG. 5A is a diagram showing a first-half LO cycle. FIG. 5B is a diagram showing a second-half LO cycle. FIG. 5C is a diagram showing resultant voltages for both of the 5A and 5B circuits.

FIGS. 6A and 6B are schematic circuit diagrams showing IF noise-shaping biquad filter. FIG. 6A is a schematic circuit diagram showing an IF noise-shaping biquad filter. FIG. 6B is a schematic circuit diagram showing a its small-signal equivalent circuit showing the noise TF of M_{f1} .

FIGS. 7A and 7B are diagrams showing impedance and noise. FIG. 7A is a diagram showing an equivalent impedance of Z_p versus ω_{op} . FIG. 7B is a diagram showing a simulated noise TF of

$$\frac{i_{n,out}}{i_{n,MF1}}$$

with and without L_{acr} .

FIG. 8 is a diagram showing simulated NF_{Total} (at $V_{o,ip}$ and $V_{o,in}$) with and without L_{acr} .

FIGS. 9A-C are diagrams showing a complex pole load, its small-signal equivalent circuit and pole plot. FIG. 9A is a schematic circuit diagram showing a complex pole load. FIG. 9B is a schematic circuit diagram showing the small-signal equivalent circuit of FIG. 9A. FIG. 9C is a diagram showing a pole plot of the circuit of FIGS. 9A and 9B.

FIG. 10 is a diagram showing simulated hybrid filter gain response.

FIGS. 11A and 11B are schematic circuit diagrams of the baseband circuitry. FIG. 11A is a schematic circuit diagram showing a VGA. FIG. 11B is a schematic circuit diagram showing a 3-stage RC-CR PPF, inverter amplifier and 50 Ω buffer.

FIG. 12 is a diagram showing simulated overall IF gain response.

FIGS. 13A-C are diagrams showing DIV1 and DIV2, and their timing diagrams. FIG. 13A is a schematic circuit diagram in block form showing divider circuits. FIG. 13B is a schematic circuit diagram showing the divider circuits. FIG. 13C is a diagram showing the timing diagrams of the circuits of FIGS. 13A and 13B.

FIGS. 14A-B are diagrams showing post layout simulations. FIG. 14A is a graphical depiction showing a post-layout simulation of NF and gain versus LO's amplitude. FIG. 14B is a schematic circuit diagram showing an additional C_{LO} generating the optimum LO's amplitude.

FIGS. 15A-C are photographic depictions of the receiver. FIG. 15A is a photomicrograph showing the receiver chip, tested under CoB and CQFP44 packaging. FIGS. 15B and C are depictions of circuit connections for the receiver chip of FIG. 15A.

FIGS. 16A-D are graphical diagrams showing measured profiles for the receiver of FIGS. 15A-C. FIG. 16A is a graphical diagram showing measured input port voltage reflection coefficient (S_{11}), FIG. 16B is a graphical diagram showing measured wide band gain and NF, FIG. 16C is a graphical diagram showing a measured $IIP3_{out-band}$. FIG. 16D is a graphical diagram showing a measured low IF filtering profile.

FIGS. 17A and 17B are graphical diagrams showing noise and input swing. FIG. 17A is a graphical diagram showing measured phase noise has enough margin to the specifications, showing that from simulations it is a tradeoff with the power budget according to the VCO's output swing. FIG. 17B is a graphical diagram showing a simulated sensitivity curve of DIV1 showing its small input voltage requirement at ~10 GHz.

DETAILED DESCRIPTION

Overview

The present disclosure describes the details of an extensive-current reuse ZigBee receiver with most RF-to-BB functions merged in one cell, while avoiding any external components for input-impedance matching. Together with a number of ULP circuits and optimization techniques, the receiver fabricated in 65 nm CMOS measures high performances in terms of IIP3, input port voltage reflection coefficient (S_{11}) bandwidth, power and area efficiencies with respect to the prior art.

In one example, a 2.4 GHz ZigBee receiver unifying a balun, a low noise amplifier (LNA) and an I/Q mixer as a unified balun LNA I/Q mixer (Blixer) and a baseband (BB) hybrid filter in one cell is fabricated in 65 nm CMOS. Without any external components, wideband input matching and passive pre-gain are concurrently achieved via co-optimizing an integrated low-Q network with a balun LNA. The latter also features active-gain boosting and partial-noise canceling to enhance the gain and noise figure (NF). Above the balun LNA are I/Q double-balanced mixers driven by a 4-phase 25% LO for down-conversion and gain phase balancing. The generated baseband currents are immediately filtered by an IF noise-shaping current mode biquad filter and a complex pole load, offering 1st-order image rejection and 3rd-order channel selection directly atop the blixer. Together with other baseband and LO circuitries, the receiver measures 8.5 dB NF, 57 dB gain and -6 dBm IIP3out-band at 1.7 mW power and 0.24 mm² die size. The input port voltage reflection coefficient (S_{11}) bandwidth (<-10 dB) covers 2.25 to 3.55 GHz being robust to packaging variations. Most performance metrics compare favorably with the state-of-the-art.

Current-Reuse Receiver Architecture

FIG. 3 is a schematic block diagram showing a RF-to-BB current-reuse ZigBee receiver. As is the case with the QLMV cell, merging the LO path with the signal path is not that desirable, as they will add noise to each other and induce signal loss. Stacking of building blocks should be in conformity with the signal flow from RF to BB, such that all bias currents serve only the signal currents. In this work, the LO path is separated, which also facilitates the use of a 25% LO for better overall performances than in its 50% counterpart. The single-ended RF input (V_{RF}) is taken by a low-Q input-matching network before reaching the balun LNA I/Q mixer, which is referred to as a "blixer". Merging the balun with the hybrid filter allows the signal to be transferred from one block to another in the current domain. Merging the balun with the hybrid filter not only saves power by sharing their bias current under a single supply, but also reduces the voltage swing at internal nodes due to the inherently low input impedance of the hybrid filter, benefiting the linearity. This avoids explicit voltage-to-current and current-to-voltage interfaces, resulting in power savings. This arrangement also reduces voltage swings at internal nodes due to the inherently low input impedance of the hybrid filter, thus benefiting the linearity. The wideband input-matching network is also responsible for the pre-gain to enhance the NF. Unlike the LMV cell that only can utilize single-balanced mixers, the balun LNA features a differential output ($\pm i_{LNA}$), which allows the use of double-balanced mixers (DBMs). The balun is driven by a 4-phase 25% LO, the I/Q double balanced mixers with a large output resistance that robustly corrects the differential imbalances of $\pm i_{LNA}$. The balanced baseband currents ($\pm i_{MIX,I}$ and $\pm i_{MIX,Q}$) are then filtered directly in the current domain by a current mode biquad filter

stacked atop the double balanced mixer. The biquad filter features in-band noise shaping centered at the desired intermediate frequency (IF, 2 MHz). Only the filtered output currents ($\pm i_{i,LPF,I}$ and $\pm i_{i,LPF,Q}$) are returned as voltages ($\pm V_{o,I}$ and $\pm V_{o,Q}$) through the complex pole load, which performs both image rejection and channel selection. As the RF to baseband functions (balun LNA, DBM and baseband filter) are stacked in one cell, the signal processing can be kept in the current domain before adequate baseband filtering for better linearity, while the whole receiver only draws one bias current or a single bias current.

Out of the current-reuse path there is a high-swing variable-gain amplifier (VGA). It essentially deals with the gain loss of its succeeding 3-stage RC-CR polyphase filter (PPF), which is responsible for large and robust image rejection over mismatches and process variations. The final stage is an inverter amplifier before 50Ω test buffering. The 4-phase 25% LO can be generated by an external 4.8 GHz reference (LO_{ext}) after a divide-by-2 (DIV1) that features 50% input 25% output, or from an integrated 10 GHz voltage controlled oscillator (VCO) after DIV1 and DIV2 (25% input 25% output) for additional testability.

Wideband Input-Matching Network

FIGS. 4A-C are diagrams showing a wideband input matching network, balun LNA and I/Q DBMs. FIG. 4A is a schematic circuit diagram showing the wideband input matching network, balun LNA and I/Q double balanced mixers (Q channel is omitted and the load is simplified as R_T). FIG. 4B is a graph showing a variation of the input port voltage reflection coefficient (S_{11}) bandwidth with bondwire inductance L_{BW} . FIG. 4C is a graph showing a Power of A_{GB} versus NF. FIGS. 5A and 5B are a schematic circuit diagram showing operation of the I-channel double balanced mixer. It inherently offers output balancing after averaging in one LO cycle as shown in their FIG. 5A is a diagram showing a first-half LO cycle. FIG. 5B is a diagram showing a second-half LO cycle. FIG. 5C is a diagram showing resultant voltages for both of the 5A and 5B circuits.

A schematic for the wideband input matching network is illustrated in FIG. 4A. A low-Q inductor (L_M) and two tapped capacitors (C_p and C_M) are employed for impedance down-conversion resonant and passive pre-gain. L_M also serves as the bias inductor for M_1 . R_p is the parallel shunt resistance of L_M . C_p stands for the parasitic capacitance from the pad and ESD diodes. R_{in} and C_{in} are the equivalent resistance and capacitance at node V_{in} , respectively. R'_{in} is the downconversion resistance of R_{in} . L_{BW} is the bondwire inductance and R_s is the source resistance. To simplify the analysis, we first omit L_{BW} and C_{in} , so that L_M , C_p , C_M , R_s and R_T ($=R_p//R_{in}$) together form a tapped capacitor facilitating the input matching. Generally, $S_{11} \leq -10$ dB is required and the desired value of R'_{in} is from 26 to 97Ω over the frequency band of interest. Thus, given the R_T and C_M values, the tolerable C_p can be derived from

$$R'_{in} = R_T \left(\frac{C_M}{C_M + C_p} \right)^2.$$

The pre-gain value ($A_{pre,amp}$) from V_{RF} to V_{in} is derived from

$$\frac{V_{in}^2}{2R_T} = \frac{V_{RF}^2}{2R_S},$$

which can be simplified as

$$A_{pre,amp} = \sqrt{\frac{R_T}{R_S}}.$$

The -3 dB bandwidth of $A_{pre,amp}$ is related to the network's quality factor (Q_n) as given by:

$$Q_n = \frac{R_T}{2\omega_0 L} = \frac{\omega_0}{2\omega_{-3dB}},$$

with

$$\omega_0 = \frac{1}{\sqrt{L_M C_{EQ}}}$$

and

$$C_{EQ} = \frac{C_M C_p}{C_M + C_p}$$

In the disclosed design

$$R_T = 150 \Psi,$$

$$C_M = 1.5 \text{ pF},$$

$$L_M = 4.16 \text{ nH},$$

$$R_p = 600 \Omega,$$

$$C_p = 1 \text{ pF and}$$

$$R_{in} = 200 \Omega,$$

$A_{pre,amp}$ has a passband gain of ~ 4.7 dB over a 2.4 GHz bandwidth (at RF=2.4 GHz) under a low Q_n of 1.

Thus, the tolerable C_p is sufficiently wide (0.37 to 2.1 pF). The low-Q L_M is extremely compact (0.048 mm²) in the layout and keeps induced parasitic capacitance to a low level (~ 260 fF, part of C_{in}) as a result of the compact layout. FIG. 4B demonstrates the robustness of input port voltage reflection coefficient (S_{11}) bandwidth against L_{BW} from 0.5 to 2.5 nH. The variation of C_{in} to S_{11} bandwidth was also taken into consideration. From simulations, the tolerable C_{in} is 300 to 500 fF at $L_{BW} = 1.5$ nH.

The correlation between the input port voltage reflection coefficient (S_{11}) bandwidth and Q_n is derived in as described below with reference to FIGS. 4A-C. FIG. 4A is a diagram showing wideband input matching network, balun LNA and I/Q double balanced mixers (Q channel is omitted and the load is simplified as RL). FIGS. 4B and 4C are graphical depictions of characteristics of the network of FIG. 4A. FIG. 4B shows variation of the input port voltage reflection coefficient (S_{11}) bandwidth with bondwire inductance L_{BW} . FIG. 4C shows power of A_{GB} versus NF.

The control voltage sources comprise complex voltage components received from a local I/O oscillator LO_{Ip}, LO_{In}, connected to each pair of transistors in combination with the other pair of diode-connected transistors (M_7 , M_8) and (M_5 , M_6) connected in parallel to source and drain connections of respective ones of the 4 transistors arranged in pairs (M_5 , M_6) and (M_7 , M_8), with an I-channel driven by Q-channel IF signals, and a Q-channel driven by I-channel IF signals, resulting in the circuit synthesizing a first order complex pole load at a positive IF (+IF) or a negative IF (-IF) for channel selection and image rejection, offering image rejection and channel selection concurrently.

$S_{11} \leq -10$ dB Bandwidth Versus the Q Factor (Q_n)

A number of ULP circuits and optimization techniques have been applied based on the input port voltage reflection coefficient (S_{11}), by comparing $S_{11} \leq -10$ dB bandwidth

versus the Q factor (Q_n) of the input-Matching Network. At the resonant frequency ω_0 , L_M can resonate perfectly with C_{EQ} and R'_{in} for an exact 50Ω . At a lower frequency $\omega = \omega_0 - \Delta\omega_L$, ($\Delta\omega_L > 0$), the imaginary part of $L_M // C_{EQ}$ is non-zero, making $R'_{in} < 50\Omega$. This imaginary part is expressed as L_{eff} and derived as follows,

$$sL_M // sC_{EQ} = \frac{sL_M}{1 + s^2 C_{EQ} L_M} \quad (A-1)$$

Let, where, and if substituted into (A-1), we will have,

$$\frac{j(\omega_0 - \Delta\omega_L)L_M}{1 - \frac{(\omega_0 - \Delta\omega_L)^2}{\omega_0^2}} \approx \frac{j(\omega_0 - \Delta\omega_L)L_M}{2 \frac{\Delta\omega_L}{\omega_0}} = L_{eff} \quad (A-2)$$

where

$$\frac{\Delta\omega_L}{\omega_0} \ll 2$$

is assumed. Here, the parallel of $|L_{eff}| // R_T$ is down-converted to $R'_{in} = 26\Omega$ by C_M and C_P , thus,

$$\frac{|L_{eff} | R_T}{|L_{eff} | + R_T} \left(\frac{C_M}{C_M + C_P} \right)^2 = 26\Omega \quad (A-3)$$

Substituting (A-2) into (A-3) and simplifying them, the normalized low-side frequency is obtained,

$$\frac{\Delta\omega_L}{\omega_0} = \frac{1}{1 + \frac{4aQ_n}{R_T - a}} \quad (A-4)$$

where

$$a = 26 \left(\frac{C_M + C_P}{C_M} \right)^2$$

Then, the whole matching bandwidth is close to twice the value derived in (A-1) if the upper-side is included. (A-4) confirms that the input port voltage reflection coefficient (S_{11}) bandwidth can be significantly extended by designing a low Q_n using the size flexibility of the inductor.

Balun LNA with Active Gain Boost and Partial Noise Canceling

The common-gate (CG) common-source (CS) balun LNA avoids a need for the use of an off-chip balun, and achieves a low NF by noise canceling, but the asymmetric CG-CS transconductances and loads make the output balancing inconsistent in the wideband. In other configurations, output balancing is achieved by scaling M_5 - M_8 with cross-connection at baseband, but that is incompatible with implementations that include a hybrid filter.

In yet other designs, an AC-coupled CS branch is introduced, along with a differential current balancer (DCB). In this arrangement, the same load is allowed for both CS and CG branches for wideband output balancing. Thus, the NF of such a balun LNA can be optimized independently. This technique is transferred to this ULP design, but only with the

I/Q double balanced mixers inherently serve as the DCB, avoiding a high voltage supply.

Again referring to FIGS. 4A-C, FIG. 4A is a detailed schematic of the wideband input matching network, balun LNA and I/Q double balanced mixers. To maximize the voltage headroom, M_1 (with $g_{m,CG}$) and M_2 (with $g_{m,CS}$) were sized with non-minimum channel length ($L=0.18 \mu\text{m}$) to lower their V_T . The AC-coupled gain stage is a self-biased inverter amplifier (A_{GB}) powered at 0.6 V (V_{DD06}) to enhance its transconductance ($g_{m,AGB}$)-to-current ratio. It gain-boosts the CS branch while creating a loop gain around M_1 to enhance its effective transconductance under less bias current (I_{BIAS}). This scheme also allows the same I_{BIAS} for both M_1 and M_2 , requiring no scaling of load (i.e., only R_L). Furthermore, a small I_{BIAS} lowers the supply requirement, making a 1.2 V supply (V_{DD12}) still adequate for the balun LNA I/Q mixer and hybrid filter, while relaxing the required LO swing (LO_{IP} and LO_{IN}). C_1 - C_3 provide for biasing and are typical metal-oxide-metal (MoM) capacitors to minimize parasitics.

The balun LNA provides partial-noise canceling as a result of the CG and CS parallel amplification. When using a simplified set of criteria, the noise induced by double balanced mixer (M_5 - M_8) and the effect of channel-length modulation can be ignored. The noise transfer function (TF) of M_1 's noise ($I_{n,CG}$) to the baseband differential output ($V_{o,IP} - V_{o,IN}$) was derived when LO_{IP} is high, and the input impedance is matched,

$$TF_{I_{n,CG}} = -\frac{1}{2}(R_L - R_{in}G_mC_S R_L)$$

where

$$G_{m,CS} = g_{m,CS} + g_{m,AGB}$$

The noise of M_1 can be fully canceled if $R_{in}G_{m,CS}=1$ is satisfied, but as analyzed in subsection III-A, $R_{in} \approx 200\Omega$ is desired for input matching at low power. Thus, $G_{m,CS}$ should be $\approx 5 \text{ mS}$, rendering the noises of $G_{m,CS}$ and R_L still significant. Device sizings for full noise cancellation of M_1 should not lead to the lowest total NF (NF_{total}). In fact, one can get a more optimized $G_{m,CS}$ (via $g_{m,AGB}$) for stronger reduction of noise from $G_{m,CS}$ and R_L , instead of that from M_1 . Although this noise-canceling principle has been used in a single-ended LNA, the output balancing was not a concern there. According to the present disclosure, the optimization process is alleviated since the output balancing (relying on M_5 - M_8) and NF (relying on A_{GB}) are decoupled. Referring to FIG. 4A, this can be seen at the section identified by M_5 - M_8 with cross-connection at baseband. The simulated NF_{total} up to the $V_{o,IP}$ and $V_{o,IN}$ nodes against the power given to the A_{GB} is given in FIG. 4C. NF_{total} is reduced from 5.5 dB at 0.3 mW to 4.9 dB at 0.6 mW, but is back to 5 dB at 0.9 mW.

NF of the Balun LNA Versus the Gain ($G_{m,CS}$) of the CS Branch

The relationship of $G_{m,CS}$ and NF_{total} is also applicable to a balun LNA. FIGS. 4B and 4C show the NF of the balun LNA versus the gain ($G_{m,CS}$) of the CS branch with A_{GB} that guide the optimization.

The NF_{total} can be reduced by increasing $g_{m,AGB}$ under fixed $g_{m,CG}$ and $g_{m,CS}$, under matched input impedance. The noises from the I/Q double balanced mixers and their harmonic-folding terms, and the resistor R_p , are excluded for simplicity. Also, the conversion gain of the active mixers is assumed to be unity. Here $G_{m,CS}$ is upsized from $G_{m0,CS}$ to $G_{m,CS} = G_{m0,CS} + \Delta G_{m,CS}$, where $G_{m0,CS}$ is the value for full noise cancellation of CG branch, i.e., $R_{in} G_{m0,CS} = 1$.

The four major noise sources considered here are the thermal noises, which are derived from:

RS: $(V_{n,RS})^2 = 4 \text{ kTR}_S$,

M1: $(I_{n,CG})^2 = 4 \text{ kT}\gamma g_{m,CG}$,

M₂+A_{GB}: $(I_{n,CS})^2 = 4 \text{ kT}\gamma g_{m,CS}$, and

R_L: $(V_{n,L})^2 = 4 \text{ kTR}_L$,

where γ is the bias-dependent coefficient of the channel thermal noise. The noise contributed by the CG branch can be deduced as,

$$\begin{aligned} NF_{G_m,CG} &= \frac{V_{n,out,CG}^2}{V_{n,out,RS}^2} \quad (B-1) \\ &= \frac{\frac{1}{4} I_{n,CG}^2 [R_L - R_{in}(G_{m0,CS} + \Delta G_{m,CS})R_L]^2}{4kTR_S A_{pre,amp}^2 \times \frac{1}{4} \times \left[\frac{R_L}{R_{in}} + (G_{m0,CS} + \Delta G_{m,CS})R_L \right]^2} \\ &= \frac{\gamma g_{m,CG} (R_{in} R_L \Delta G_{m,CS})^2}{R_S A_{pre,amp}^2 \left(\frac{2R_L}{R_{in}} + \Delta G_{m,CS} R_L \right)^2} \\ &\approx \frac{\gamma g_{m,CG} (R_{in}^4 (\Delta G_{m,CS})^2)}{4A_{pre,amp}^2 R_S} \end{aligned}$$

$$\text{where } \frac{2R_L}{R_{in}} \gg \Delta G_{m,CS} R_L$$

If $\Delta G_{m,CS}$ is increased, the noise from M1 also moves up. For the noise contribution of the CS branch, we can derive its TF to the output (V_{out}) as,

$$TF_{G_m,CS \rightarrow V_{out}} = \frac{R_L}{1+T} \left[\frac{T}{R_{in}(G_{m0,CS} + \Delta G_{m,CS})} + 1 \right] \approx R_L(1 - \Delta G_{m,CS} R_{in})$$

where T is the loop gain $\gg 1$. With it, the NF of and NF of RL can be derived,

$$\begin{aligned} NF_{G_m,CG} &= \frac{V_{n,out,CS}^2}{V_{n,out,RS}^2} = \frac{4kT\gamma(G_{m,CS} + \Delta G_{m,CS})(TF_{G_m,CS \rightarrow V_{out}})^2}{4kTR_S A_{pre,amp}^2 \times \frac{1}{4} \times \left[\frac{2R_L}{R_{in}} + \Delta G_{m,CS} R_L \right]^2} \quad (B-2) \\ &\approx \frac{\gamma R_{in}^2 (G_{m0,CS} + \Delta G_{m,CS})(1 - \Delta G_{m,CS} R_{in})^2}{R_S A_{pre,amp}^2 R_S} \\ &\approx \frac{\gamma R_{in}^4 (1 - \Delta G_{m,CS} R_{in})^2}{R_S A_{pre,amp}^2} \end{aligned}$$

$$\text{where } \frac{2R_L}{R_{in}} \gg \Delta G_{m,CS} R_L$$

With it, the NF of $G_{m,CS}$ and NF of R_L can be derived, then

$$\begin{aligned} NF_{R_L} &= \frac{4kTR_L}{4kTR_S A_{pre,amp}^2 \times \frac{1}{4} \times \left[\frac{R_L}{R_{in}} + (G_{m,CS} + \Delta G_{m,CS})R_L \right]^2} \quad (B-3) \\ &\approx \frac{4R_L}{R_S A_{pre,amp}^2} \times \frac{1}{\left(\frac{4R_{in}^2}{R_{in}^2} + \frac{2\Delta G_{m,CS} R_L^2}{R_{in}} \right)} \end{aligned}$$

-continued

$$\approx \frac{R_{in}^2}{R_L R_S A_{pre,amp}^2} \times \left(1 - \frac{\Delta G_{m,CS} R_{in}}{2} \right)$$

As expected, when $\Delta G_{m,CS}$ is increased the noise contribution of $G_{m,CS}$ and R_L can be reduced. The optimal $\Delta G_{m,CS}$ can be derived from

$$\frac{\partial NF_{total}}{\partial \Delta G_{m,CS}} = 0,$$

$$\text{where } NF_{total} = 1 + NF_{G_m,CG} + NF_{G_m,CS} + 2NF_{R_L}$$

Double-Balanced Mixers Offering Output Balancing

The active-gain-booster balun LNA can only generate unbalanced outputs. The output balancing is inherently performed by the I/Q double balanced mixers under a 4-phase 25% LO. For simplicity, this principle is described for the I channel only under a 2-phase 50% LO, as shown in FIGS. 5A and 5B, where the load is simplified as R_L. During the first-half LO cycle when LO_{Ip} is high, i_{LNAp} goes up and appears at V_{o,Ip} while i_{LNAi} goes down and appears at V_{o,Ii}. In the second-half LO cycle, both of the currents' sign and current paths of i_{LNAp} and i_{LNAi} are flipped. Thus, when they are summed at the output during the whole LO cycle, a robust output balance is obtained. The output balancing is robust, due to the large output resistance (9 kΩ) of M₅-M₈ enabled by the very small I_{Bias} (85 μA). To analytically prove the principle, we let

$$i_{LNAp} = \alpha I_A \cos(\omega_s t + \omega_1)$$

and

$$i_{LNAi} = -I_A \cos(\omega_s t + \phi_2) \times \cos \omega_0 t,$$

where I_A is the amplitude,

ω_s is the input signal frequency,

α is the unbalanced gain factor and ϕ_1 and ϕ_2 are their arbitrary initial phases.

When there is sufficient filtering to remove the high-order terms, we can deduce the baseband currents $i_{MIX,Ip}$ and $i_{MIX,Ii}$ as given by,

$$\begin{aligned} i_{MIX,Ip} &= \frac{2}{\pi} \alpha I_A \cos(\omega_s t + \phi_1) \times \cos \omega_0 t + \frac{2}{\pi} I_A \cos(\omega_s t + \phi_2) \times \cos \omega_0 t \quad (2) \\ &= \frac{\alpha I_A}{\pi} \cos(\omega_s t + \omega_0 t + \phi_1) + \frac{I_A}{\pi} \cos(\omega_0 t - \omega_s t + \phi_2) \end{aligned}$$

so

$$\begin{aligned} i_{MIX,Ii} &= \frac{I_A}{\pi} \cos(\omega_s t + \omega_0 t + \phi_2) + \frac{\alpha I_A}{\pi} \cos(\omega_0 t - \omega_s t + \phi_1) \quad (3) \\ &= -i_{MIX,Ip} \end{aligned}$$

From the deduced baseband currents, a consistent proof for I/Q double balanced mixers under a 4-phase 25% LO is obtained. Ideally, from (2)-(3), the double balanced mixer can correct perfectly the gain and phase errors from the balun LNA, independent of its different output impedances from the CG and CS branches. In fact, even if the conversion gain of the two mixer pairs (M₅, M₈ and M₆, M₇) does not match (e.g., due to non-50% LO duty cycle), the double-balanced operation can still generate balanced outputs (confirmed by simulations). Of course, the output impedance of the double balanced mixer can be affected by that of the

balun LNA, as shown in FIG. 4A, but is highly desensitized by employing a small size R_L (i.e., the input impedance of the hybrid filter) originally aimed for current mode operation. Thus, the intrinsic imbalance between $V_{o,ip}$ and $V_{o,in}$ is negligibly small (confirmed by simulations).

For devices sizing, a longer channel length ($L=0.18 \mu\text{m}$) is preferred for M_{5-8} to reduce their $1/f$ noise and V_T . Hard-switch mixing helps to desensitize the I/Q double balanced mixers to LO gain error, leaving the image rejection ratio (IRR) mainly determined by the LO phase error that is a tradeoff with the LO-path power. Here, the targeted LO phase error is relaxed to $\sim 4^\circ$, as letting the baseband circuitry (i.e., the complex pole load and 3-stage RC-CR PPF) to handle the IRR is more power efficient, as detailed in Sections III-E and III-F. The resultant voltages are shown in FIG. 5C.

Hybrid Filter Biquad Filter with IF Noise-Shaping

FIGS. 6A and 6B are schematic diagrams showing a hybrid filter first half current mode biquad filter with IF noise-shaping. FIG. 6A shows the biquad filter and FIG. 6B shows its small-signal equivalent circuit. The equivalent circuit in FIG. 6B shows the noise TF of M_{j1} . In FIG. 6A, a set of four transistors M_{j1} - M_{j2} , are connected in a parallel-series connection with transistors M_{j1} , M_{j2} cross-connected at the series connection. Also depicted is the active inductor in which M_{i1} - M_{i4} are series-parallel connected with each of M_{j1} - M_{j4} cross-connected to their opposite series connections.

The current mode biquad filter shown in FIG. 6A is an excellent candidate for current-reuse with the balun LNA I/Q mixer for channel selection. This biquad filter only can generate a noise-shaping zero spanning from DC to $\sim 2\pi \cdot 0.1Q_B\omega_{0B}$ MHz for M_{j1} - M_{j2} , where Q_B and ω_{0B} are the biquad filter's quality factor and -3 dB cutoff frequency, respectively. This noise shaping is hence ineffective for the disclosed low-IF design having a passband from ω_1 to ω_2 ($=\omega_{0B}$), where $\omega_1 > 0.1Q_B\omega_{0B}$. To address this issue, an active inductor (L_{act}) is added at the sources of M_{j1} - M_{j2} . The $L_{act}C_{j1}$ resonator shifts the noise-shaping zero to the desired IF. If, as in the usual case, such an IF is in range of MHz, L_{act} cannot be achieved by a passive inductor as it will be prohibitively large in size. The cross-diode connection between M_{i1} - M_{i4} (all with $g_{m,act}$) emulate $L_{act} \approx C_{j1}/g_{m,act}^2$. The small-signal equivalent circuit to calculate the noise TF of $i_{n,Mj1}/i_{n,out}$ is shown in FIG. 6B.

FIGS. 7A and 7B are graphical diagrams showing characteristics of the biquad filter. FIG. 7A shows equivalent impedance of ZP versus ω_{or} . FIG. 7B shows simulated noise TF of

$$\frac{i_{n,out}}{i_{n,Mj1}}$$

with and without L_{act} . An approximated impedance of Z_P in different frequencies related to ω_{or} is summarized in FIG. 7A, where

$$\omega_{or} = \frac{\omega_1 + \omega_2}{2}$$

is the resonant frequency of $L_{act}C_{j1}$ at IF. The simulated $i_{n,Mj1}/i_{n,out}$ is shown in FIG. 7B. At the low frequency range, Z_P behaves inductively, degenerating further $i_{n,Mj1}$ when the frequency is increased. At the resonant frequency, $Z_P=R_{sf}$

where R_{sf} is the parallel impedance of the active inductor's shunt resistance and double balanced mixer's output resistance. The latter is much higher when compared with R_L thereby suppressing $i_{n,Mj1}$. At the high frequency range, Z_P is more capacitive dominated by C_{j1} . It implies $i_{n,Mj1}$ can be leaked to the output via C_{j1} , penalizing the in-band noise. At even higher frequencies, the output noise decreases due to C_{j2} , being the same as its original form.

FIG. 8 is a graphical diagram showing simulated NF_{Total} (at $V_{o,ip}$ and $V_{o,in}$) with and without L_{act} . The signal TF can be derived from FIG. 8. Here

$$R_L = \frac{1}{g_{mf}}, L_{biq} = \frac{C_{f2}}{G_{mf}^2}$$

For an effective improvement of NF, $L_{act} \gg L_{biq}$ should be made. The simulated NF_{total} at $V_{o,ip}$ and $V_{o,in}$ with and without the L_{act} is shown FIG. 8, showing about ~ 0.1 dB improvement (reasonable contribution for a baseband circuit). Here M_{j1} - M_{j4} use isolated P-well for bulk-source connection, avoiding the body effect while lowering their V_T .

Hybrid Filter 2nd Half—Complex Pole Load

Unlike most active mixers or the original balun LNA I/Q mixer that only use a RC load, the proposed "load" synthesizes a first order complex pole at the positive IF (+IF) for channel selection and image rejection. FIGS. 9A-C are diagrams showing a complex pole load, its small-signal equivalent circuit and pole plot. FIG. 9A is a schematic circuit diagram showing a complex pole load. FIG. 9B is a schematic circuit diagram showing the small-signal equivalent circuit of FIG. 9A. FIG. 9C is a diagram showing a pole plot of the circuit of FIGS. 9A and 9B.

FIG. 10 is a diagram showing simulated hybrid filter gain response. The circuit implementation and principle are shown in FIGS. 9A and 9B, respectively. The real part (R_L) is obtained from the diode-connected M_L , whereas the imaginary part ($g_{m,Mc}$) is from the I/Q cross-connected M_C . The entire hybrid filter, such as shown in FIG. 7A and in FIG. 9B, offers 5.2 dB IRR, and 12 dB (29 dB) adjacent (alternate) channel rejection as shown in FIG. 10 (the channel spacing is 5 MHz). Similar to g_m -C filters the center frequency is defined by $g_{m,Mc}R_L$. When sizing the -3 dB bandwidth, the output conductances of M_C and M_L should be taken into account.

Current-Mirror VGA and RC-CR PPF

FIGS. 11A and 11B are schematic circuit diagrams of the baseband circuitry. FIG. 11A is a schematic circuit diagram showing a VGA. FIG. 11B is a schematic circuit diagram showing a 3 stage RC CR PPF, inverter amplifier and 50 Ω buffer. Outside the current-reuse path, $V_{o,I}$ and $V_{o,Q}$ are AC-coupled to a high swing current-mirror VGA formed with M_L shown in FIG. 9A and a segmented M_{VGA} as shown in FIGS. 11A and 11B, offering gain controls with a 6 dB step size. To enhance the gain precision, the bias current through M_{VGA} is kept constant, so as its output impedance. With the gain switching of M_{VGA} , the input-referred noise of M_{VGA} will vary. However, when the RF signal level is low the gain of the VGA should be high, rendering the gain switching not influencing the receiver's sensitivity. The VGA is responsible for compensating the gain loss (30 dB) of the 3-stage passive RC-CR PPF that provides robust image rejection of >50 dB (corner simulations). With the hybrid filter rejecting the out-band blockers the linearity of

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the VGA is further relaxed, so as its power budget (192 μ W, limited by the noise and gain requirements).

A 3-stage RC-CR PPF can robustly meet the required IRR in the image band (i.e., the -1F), and cover the ratio of maximum to minimum signal frequencies. In the disclosed design, the expected IRR is 30 to 40 dB and the ratio of frequency of the image band is $f_{max}-f_{min}$ (=3). Counting the RC variations as large as $\pm 25\%$, the conservative $\Delta f_{eff}=f_{max_eff}/f_{min_eff}$ should be close to 5:

$$\frac{\sigma(\text{UImage Out})}{\text{Desired Out}} = 0.25 \sqrt{\left(\frac{\sigma_R}{R}\right)^2 \left(\frac{\sigma_C}{C}\right)^2} \quad (4)$$

Accordingly, the matching of the resistors (σ_R) and capacitors (σ_C) can be relaxed to 0.9% (2.93%) for 40 dB (30 dB) IRR with a 3σ yield. Here, ~ 150 k Ω resistors are chosen to ease the layout with a single capacitor size (470 fF), balancing the noise, area and IRR. The simulated worst IRR is 36 dB without LO mismatch, and still over 27 dB at a 4° LO phase error checked by 100x Monte Carlo simulations. Furthermore, if the 5 dB IRR offered by the complex pole load is added the minimum IRR of the IF chain should be 32 dB. The final stage before 50 Ω output buffering is a self-biased inverter amplifier (power=144 μ W), which embeds one more real pole for filtering.

FIG. 12 is a diagram showing simulated overall IF gain response. The simulated overall IF gain response is shown in FIG. 12, where the notches at DC offered by the AC-coupling network, and around the -1F offered by the 3-stage RC-CR PPF, are visible. The IRR is about 57 dB under an ideal 4-phase 25% LO for the image band from ($f_{LO}-3$, $f_{LO}-1$) MHz. (57 dB=52 dB (RC-CR PPF)+5 dB, as a complex pole load.)

VCO and Dividers and LO Buffers

To fully benefit the speed and low- V_T advantages of fine line-width CMOS, the entire LO path is powered at a lower supply of 0.6 V to reduce the dynamic power. For additional testability, an on-chip VCO is integrated. It is optimized at ~ 10 GHz to save area and allows division by 4 for I/Q generation. The loss of its LC tank is compensated by complementary nmOS-PMOS negative transconductors.

FIGS. 13A-C are diagrams showing DIV1 and DIV2, and their timing diagrams. FIG. 13A is a schematic circuit diagram in block form showing divider circuits. FIG. 13B is a schematic circuit diagram showing the divider circuits. FIG. 13C is a diagram showing the timing diagrams of the circuits of FIGS. 13A and 13B.

The divider chain shown in FIG. 13A cascades two types of divide-by-2 circuits (DIV1 and DIV2) to generate the desired 4-phase 25% LO, from a 2-phase 50% output of the VCO. The two latches (D1 and D2) are employed to build DIV1 that can directly generate a 25% output from a 50% input, resulting in power savings due to less internal logic operation (i.e., AND gates) and load capacitances. Each latch consists of two sense devices, a regenerative loop and two pull up devices. For 25% input 25% output division, DIV2 is proposed that it can be directly interfaced with DIV1. The 25% output of DIV1 are combined by M_{D1} to M_{D4} to generate a 50% clock signal for D3 and D4.

For testing under an external LO_{ext} source at 4.8 GHz, another set of D1 and D2 is adopted. The output of these two sets of clocks are combined by transmission gates and then selected. Although their transistor sizes can be reduced aggressively to save power, their drivability and robustness in process corners can be degraded. From simulations, the

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sizing can be properly optimized. The four buffers (Buf₁-Buf₄) serve to reshape the pulses from DIV2 and enhance the drivability. The timing diagram is shown in FIG. 13B.

FIGS. 14A-B are diagrams showing post layout simulations. FIG. 14A is a graphical depiction showing a post-layout simulation of NF and gain versus LO's amplitude. FIG. 14B is a schematic circuit diagram showing an additional C_{LO} generates the optimum LO's amplitude. Due to the very small I_{BLAS} for the I/Q double balanced mixers, a LO amplitude of around $0.4 V_{pp}$ is found to be more optimized in terms of NF and gain as simulated and shown in FIG. 14A. To gain benefits from it C_{LO} is added to realize a capacitor divider with $C_{MLX,in}$ (input capacitance of the mixer) as shown in FIG. 14B. This act brings down the equivalent load ($C_{L,eq}$) of Buf₁-Buf₄ by $\sim 33\%$.

Experimental Results

FIGS. 15A-C are photographic depictions of the receiver. FIG. 15A is a photomicrograph showing the receiver chip, tested under CoB and CQFP44 packaging. FIGS. 15B and C are depictions of circuit connections for the receiver chip of FIG. 15A. The ZigBee receiver was fabricated in 65 nm CMOS and optimized with dual supplies (1.2 V: balun LNA I/Q mixer+hybrid filter, 0.6 V: LO and baseband circuitries). The die area is 0.24 mm² (0.3 mm²) without (with) counting the LC-tank VCO.

FIGS. 16A-D are graphical diagrams showing measured profiles for the receiver of FIGS. 15A-C. FIG. 16A is a graphical diagram showing measured the input port voltage reflection coefficient (S_{11}), FIG. 16B is a graphical diagram showing measured wide band gain and NF, FIG. 16C is a graphical diagram showing a measured IIP3_{out-band}. FIG. 16D is a graphical diagram showing a measured low IF filtering profile. Since there is no frequency synthesizer integrated, the results in FIG. 16A-D were measured under LO_{ext} for accuracy and data repeatability. S_{11} -BW (< -10 dB) is ~ 1.3 GHz for both chip-on-board (CoB) and CQFP-packaged tests, as shown in FIG. 16A, which proves its immunity to board parasitics and packaging variations. The gain (55 to 57 dB) and NF (8.3 to 11.3 dB) are also wideband consistent, as shown in FIG. 16B. The gain peak at around 2.4 to 2.5 GHz is from the passive pre-gain. Following a linearity test profile, two tones at [LO+12 MHz, LO+22 MHz] are applied, measuring an IIP3_{out-band} of -6 dBm, as shown in FIG. 16C, at the maximum gain of 57 dB. This high IIP3 is due to the direct current mode filtering at the mixer's output before signal amplification. The asymmetric IF response, as shown in FIG. 16D shows 22 dB (43 dB) rejection at the adjacent (alternate) channel, and 36 dB IRR. The filtering rejection profile is around 80 dB/decade. The spurious free dynamic range (SFDR) is close to 60 dB,

$$SFDR = \frac{2(P_{IIP3} + 174 \text{ dBm} - NF - 10 \log BW)}{3} - SNR_{min} \quad (5)$$

where $SNR_{min}=4$ dB is the minimum signal-to-noise ratio required by the application, and $BW=2$ MHz is the channel bandwidth.

The receiver was further tested at lower voltage supplies as summarized in Table I:

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TABLE I

Key performances of the receiver at different supply voltages.			
Supply Voltage (V)	0.6/1.2	0.6/1	0.5/1
Power (mW)	1.7	1.2	0.8
Gain (dB)	57	58	57.5
IIP3 _{out-band} (dBm)	-6	-4	-8
NF (dB)	8.5	11.3	12
IRR (dB)	36	38	35

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that has an enough margin to the specifications as shown in FIG. 17A. Porting it to the simulation results, it can be found that the corresponding VCO's output swing is $0.34 V_{pp}$ and the total LO-path power is 1.7 mW (VCO+dividers+BUFs). Such an output swing is adequate to lock DIV1 as shown in its simulated sensitivity curve, as shown in FIG. 17B.

The chip summary and performance benchmarks are given in Table II, showing current-reuse architectures, a classical architecture with cascade of building blocks, and an ultra-low-voltage design. The results measured under a 10 GHz on-chip VCO are also included for completeness, but they are more sensitive to test uncertainties:

TABLE II

Performance summary and benchmark with the state-of-the-art.					
	This Disclosure	JSSC'10 [7]	JSSC'10 [8]	JSSC'10 [23]	ISSCC'13 [5]
Application	ZigBee	ZigBee	GPS	ZigBee/Bluetooth	Energy Harvesting
Architecture	Blixer + Hybrid-Filter + Passive RC-CR PPF	LMV Cell + Complex Filter	QLMV Cell + Complex Filter	LNA + Mixer + Complex Filter	LNA + Mixer + Frequency-translated IF Filter
BB Filtering	1 Biquad + 4 complex poles zero	3 complex poles	2 complex poles	3 complex poles	2 real poles
External I/P Matching Components		1 inductor, 1 capacitor	1 passive balun	1 inductor, 1 capacitor	2 capacitors, 1 inductor
$S_{11} < -10$ dB	1300	<300	100	>400	>600
Bandwidth (MHz)	(2.25 to 3.55 GHz)	(2.3 to 2.6 GHz)	(1.55 to 1.65 GHz)	(<2.2 to 2.6 GHz)	(<2 to 2.6 GHz)
Integrated VCO	No	Yes	Yes	No	Yes
Gain (dB)	57	55	75	67	83
Phase Noise (dBc/Hz)	NA	-115 @ 3.5 MHz	-116 @ 3.5 MHz	-110 @ 1 MHz	-112.8 @ 1 MHz
NF (dB)	8.5	9	9	16	6.1
IIP3 _{out-band} (dBm)	-6	-6	-12.5	N/A	-21.5
IRR (dB)	36 (worst of 5 chips)	28	35	32	N/A
SFDR (dB)	60.3	60	55.5	N/A	53.6
LO-to-RF Leak (dBm)	-61	-61	-60	-75	N/A
Power (mW)	1.7*	2.7	3.6	6.2 (inc. ADC)	20
Active Area (mm ²)	0.24	0.3	0.35	1.5 (inc. ADC)	1.45
Supply Voltage (V)	0.6/1.2	1.2	1	0.6	0.3
Technology	65 nm CMOS	90 nm CMOS	130 nm CMOS	65 nm CMOS	65 nm CMOS

*Breakdown: 1 mW: Blixer + hybrid filter + BB circuitry, 0.7 mW: DIV1 + LO Buffers

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Only the NF degrades more noticeably, the IIP3, IRR and BB gain are almost secured. The better IIP3 for 0.6 V/1-V operation is mainly due to the narrower -3 dB bandwidth of the hybrid filter. For the 0.5 V/1-V operation, the degradation of IIP3_{out-band} is likely due to the distortion generated by A_{GB} . Both cases draw very low power down to 0.8 mW, being comparable with other ULP designs.

The LC-tank VCO was tested separately. FIGS. 17A and 17B are graphical diagrams showing noise and input swing of the LC-tank VCO. FIG. 17A is a graphical diagram showing measured phase noise has enough margin to the specifications, showing that from simulations it is a tradeoff with the power budget according to the VCO's output swing. FIG. 17B is a graphical diagram showing a simulated sensitivity curve of DIV1 showing its small input voltage requirement at -10 GHz. The power budget of the LC-tank VCO is related with its output swing and is a tradeoff with the phase noise, which measures 114 dBc/Hz at 3.5 MHz

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The degraded NF and IRR are mainly due to the phase noise of the free-running VCO. In both cases, this work succeeds in advancing the IIP3_{out-band}, power and area efficiencies, while achieving a wideband input port voltage reflection coefficient (S_{11}) with zero external components. As compared with similar systems, the presently disclosed technology achieves 8x less area and 15.5 dBm higher IIP3, together with stronger baseband channel selectivity.

CONCLUSION

A number of ULP circuits and optimization techniques have been applied to the design of a 2.4 GHz ZigBee receiver in 65 nm CMOS. The extensive-current-reuse RF-to-BB path is based on a balun LNA I/Q mixer+hybrid filter topology, which improves not only the power and area efficiencies, but also the out-band linearity due to more current-domain signal processing. Specifically, the balun LNA I/Q mixer features: 1) a low-Q input matching network realizing wideband input port voltage reflection coefficient (S_{11}) and robust passive pre-gain, 2) a balun LNA with

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active-gain boosting and partial-noise canceling improving the gain and NF, 3) I/Q double balanced mixers driven by a 4-phase 25% LO inherently offering output balancing. For the hybrid filter, an IF noise-shaping biquad filter together with a complex pole load synthesizes 3rd-order channel selection and 1st-order image rejection. All of them render current-reuse topologies with great potential for developing ULP radios in advanced CMOS processes.

It will be understood that many additional changes in the details, materials, steps and arrangement of parts, which have been herein described and illustrated to explain the nature of the subject matter, may be made by those skilled in the art within the principle and scope of the invention as expressed in the appended claims.

What is claimed is:

1. A complex pole load comprising:

a parallel circuit comprising 8 transistors arranged in four pairs, with each pair receiving filtered output currents

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from a biquad filter circuit as an input to conduct I and Q current, respectively, in the pairs, each pair of transistors comprising a transistor in one pair gated by control voltage sources, connected in parallel with a transistor diode connected for gating by the respective input of a transistor in the other pair, and the control voltage sources comprising complex voltage components, with an I channel driven by Q channel IF signals, and a Q channel driven by I channel IF signals, resulting in the circuit synthesizing a first order complex pole load at a positive IF (+IF) or a negative IF (IF) for channel selection and image rejection, offering image rejection and channel selection concurrently.

2. The IF-noise-shaping transistorized current-mode low-pass filter of claim 1, further comprising: a second set of circuit elements, thereby separately applying the pole loads to I and Q complex signals.

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