A Two-Channel Time-Interleaved Continuous-Time Third-Order CIFF-Based Delta-Sigma Modulator

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***Abstract*— This work introduces a two-channel time-interleaved (TI) continuous-time (CT) 3rd-order delta-sigma modulator (DSM). It uses the information from one complete channel to predict the other channel based on the extrapolation principle. Note that, Cascaded Integrator of Distributed Feedforward (CIFF) topology is selected for the loop filter for the following reasons: 1) it could reduce the number of required feedback DACs as much as possible; 2) it allows to implement the zero optimization for the TI DSM such that the performance could be further improved. Furthermore, we employ the technique of error correction to address the issue regarding the delay-free feedback path, which originates from the extrapolating TI DSM. We present the derivations of the target TI CT DSM starting from a single-channel discrete-time (DT) DSM, while the compensation for excess loop delay (ELD) is considered. Fabricated in 65nm CMOS process, this modulator achieves an equivalent output sampling rate of 800MS/s, while the analog channel operates at 400MHz. It exhibits a signal-to-noise and distortion ratio (SNDR) /spurious-free dynamic range (SFDR)/dynamic range (DR) of 75.5dB/89.7dB/79dB over a 10MHz bandwidth. The total power consumption is 33.73mW from 1.2v/1.8v power supplies. It results in a Schreier Figure of Merit (FoM) of 163.7dB based on DR.**

***Index Terms*— Continuous-time delta-sigma modulator (DSM), time-interleaved (TI), cascaded integrator of distributed feedforward (CIFF), excess loop delay (ELD) compensation.**

I. Introduction

CONTINUOUS time (CT) delta sigma modulators (DSM) are widely used in a wireless high-sensitivity receiver, as they could achieve a high dynamic range (DR) while featuring some special system-level advantages, such as inherent antialiasing filtering and resistive input impedance [1], [2], [3], [4], [5], [6]. In order to achieve a high DR of a CT DSM, the methods can be considered as the following aspects: 1) increase the order of the loop filter, however, it comes with the stability concern; 2) increase the bit-width of the quantizer, but the resolution is generally chosen within 5bit due to the complexity concern; 3) increase the oversampling ratio (OSR), but the usable OSR is restrained as the maximum operating frequency of a single DSM loop is limited by the regeneration time of the quantizer (QTZ), the transition rate of the DAC, the finite bandwidth (BW) of the operational amplifier, etc.

Time-interleaving (TI) technique provides an alternative to increasing the equivalent OSR of the noise-shaping ADCs [7], [8], [9], [10], [11], [12]. Moreover, owing to the oversampling, the artifacts induced by the channel mismatch fall out of the band of interest. It means that the TI DSM is inherently insensitive to the channel mismatch as being critical in the Nyquist-rate ADC. Nevertheless, owing to the recursive operation of the DSM, the TI DSM requires to generate the complicated feedback signals as well as the integrator outputs, which makes it more complicated compared to the TI Nyquist-rate ADCs [11]. It accounts for why the majority of TI implementations are Nyquist-rate ADCs. Therefore, the development of TI DSMs leads to the exploration of simple circuit implementation.

To implement a TI DSM, the straightforward way is to directly parallel N sub-DSMs while introducing the cross-coupling paths [7]. However, such TI DSM suffers from the duplicated hardware and cross-coupling complexity. Moreover, the mismatch between the global DAC feedback (from each channel) can be also problematic [11]. Alternatively, since the integrator is a memory element, the extrapolation technique allows to predict the output of other channel by using the node information (e.g. the input signal, the integrator output) of the known channel. As a result, the complexity of the TI DSM could be significantly reduced. Thereby, the extrapolation-based TI DSM has become the main stream to be explored, either in discrete-time (DT) or CT domains [9], [10], [11], [12]. Note that the extrapolation is naturally completed in the analog domain. However, as the number of TI channels increases, the inherent recursive iterations would lead to extremely large extrapolation gains in the analog domain, thus making the circuitry-level implementation infeasible. Instead, with the help of digital feedforward paths, the extrapolation could be implemented in the digital domain, resulting in a four-channel (4x) TI DSM [9]. Nevertheless, large extrapolation gains would amplify the quantization noise (QN)

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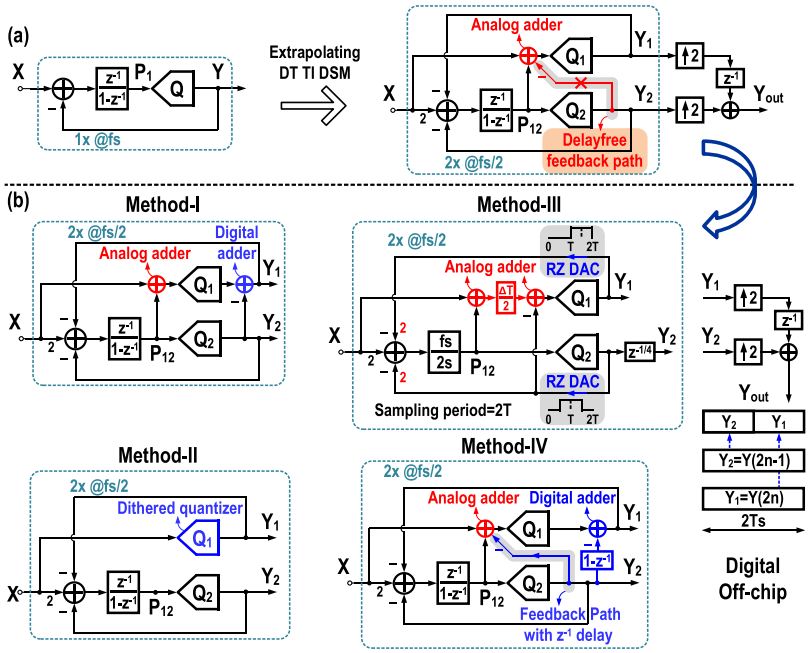

Fig. 1. (a) Transformation from a basic 1st-order DSM to extrapolating 2x TI DT DSM. (b) four methods addressing the delay-free feedback path.

simultaneously in the digital domain, thus resulting in QN penalty as high as ~26dB [9]. On the other hand, CT DSMs using TI quantizers have been explored [4]. Using TI quantizer can be effective to alleviate speed requirement of quantizer. However, other key blocks of the CT DSM, such as DACs and integrators, still work at a normal clock rate. Additionally, note that the TI quantizer would result in excess loop delay (ELD) exceeding a clock cycle, which poses significant challenge on the loop stability [4]. In contrast, a TI DSM can effectively reduce the clock rate for each sub-DSM at the price of a complicated loop filter, thus alleviating the speed requirement for each block as well as the ELD.

To alleviate the complexity of loop filter, this work exploits a 2x TI 3rd-order CT DSM based on the analog extrapolation, where a complete Cascaded Integrator of Distributed Feed-forward (CIFF)-based single channel is used to generate an equivalent 2x TI system. To the best of the authors' knowledge, this is the first fabricated TI 3rd-order CT DSM based on CIFF architecture. By using the CIFF topology, the zero optimization could be successfully implemented for a TI DSM system (more details would be shown in Section III-C). By using the node information of one complete channel, the QTZ input of the extended channel is predicted based on the extrapolation concept. As a result, only three integrators can implement an equivalent 2x TI 3rd-order DSM. Furthermore, to complete the DT-to-CT conversion, various loop filters of the original 2x TI DT DSM are recognized and further converted into their CT counterparts by using impulse invariant transformation, while the compensation for the excess loop delay (ELD) is considered. Operating at 400MHz, the proposed 2x TI CT DSM achieves an equivalent sampling rate of 800MHz. It achieves a signal-to-noise and distortion ratio (SNDR) of 75.5dB, a spurious-free dynamic range (SFDR) of 89.7dB and a dynamic range (DR) of 79dB over a 10MHz BW.

This paper is organized as follows. Section II introduces the extrapolating TI DSM principle, the issue regarding delay-free feedback path and the DT-to-CT conversion of TI DSM architecture. Section III presents the proposed TI architecture. Section IV depicts the circuitry implementation, followed by the measurement results included in Section V. Finally, Section VI concludes this paper.

II. Time-Interleaving Techniques of CT DSM

A. Extrapolating TI DT DSM

As aforementioned, the prior arts confirm that the technique of extrapolation leads to a relatively simple circuitry-level implementation. The extrapolation relies on the fact that a TI DSM incorporates memory elements in the loop filter, and the expected next sample is highly related to the previous samples [11], [12]. Thereby, it is feasible to use the information of one known channel to extrapolate (or predict) the outputs of other channels. Next, we will take a 1st-order DT DSM as an example to demonstrate how its 2x TI structure is constructed. Note that the noise transfer function (NTF) of a basic 1st-order DT DSM is $1\text{-}z^{-1}$. Owing to the recursive operation, the desired loop filter of 2x TI 1st-order DT DSM is given by [9],

$$H(z) = \begin{bmatrix} z^{-1} & 1 \\ z^{-1} & z^{-1} \end{bmatrix} \times \frac{1}{1 - z^{-1}} \tag{1}$$

Due to the oversampling property, we could make the input X approximately equal to the input of each channel (input extrapolation), without requiring the input sampler as Nyquist-rate ADCs. As observed in Fig. 1 (top right), the output Y_1 of the extrapolating channel and the output Y_2 of the known channel can be expressed as Eq. (2. a) and Eq. (3). Note that Eq. (2. b) and Eq. (2. c) are equivalent transformations from

Eq. (2. a), both of which would be explained later. Note that Y_2 signal is discrete-time signal from the second QTZ and both QTZs have the same LSB. Therefore, there is no difference whether Y_2 signal is placed before the 1st QTZ or behind it.

$$Y_1[n] = Q_1[X[n] - Y_2[n] + P_{12}[n]] \quad (2.\text{ a})$$
$$= Q_1[X[n] + P_{12}[n]] - Y_2[n] \quad (2.\text{ b})$$
$$= Q_1[X[n] - Y_2[n-1] + P_{12}[n]] - (Y_2[n] - Y_2[n-1]) \quad (2.\text{ c})$$
$$Y_2[n] = Q_2[P_{12}[n]] \quad (3)$$

As depicted in Eq. (2. a), it requires a delay-free feedback path, where the output of the 2nd QTZ (Q_2) is directly given into the extrapolating channel as illustrated in Fig. 1 (cf. top right). Such delay-free path makes the implementation of an extrapolating TI DSM impractical. Current solutions to this issue would be discussed in the next part.

B. Solutions of Delay-Free Feedback Path

Fig. 1(b) lists four methods to solve the delay-free feedback path, described as Method-I, Method-II, Method-III and Method-IV, respectively. Their advantages and disadvantages are analyzed as follows.

1) Corresponding to Eq. (2. b), Method-I moves the delay-free feedback path into the digital domain, instead of performing it in the analog domain. However, without the feedback signal from the output (i.e. Y_2) of the known channel, the input amplitude of the QTZ (i.e. Q_1) of the extrapolation channel will become large. It disadvantageously impairs the achievable maximum stable amplitude (MSA).

2) Furthermore, as depicted as Method-II, a digital feedforward extrapolation technology is proposed in paper [9], which migrates all required extrapolating gains and adders into the digital domain, thus reducing the power and area overhead. However, owing to the digital feedforward operation, the QN is amplified a lot during the digital extrapolation process. Due to such QN penalty, the achievable signal-quantization-noise ratio (SQNR) of 4x TI DSM (4∗Fs) is almost the same as that of the single-channel DSM with a clock rate of Fs. Moreover, digital feedforward paths need to digitize the information from all nodes. As expected, as the loop order increases, the number of the required QTZs would be increased as well as the additional QN penalty. Hence, this may limit the loop order using such a digital feedforward extrapolation technique.

3) Method-III shows how to address the issue of the delay-free feedback path in 2x TI CT DSM [13]. It separates the sampling instant of two QTZs while using the return-to-zero (RZ) DAC to allow such timing allocation. Moreover, a sample-and-hold circuit is required to hold the signal until the DAC feedback signal from the 2nd QTZ (i.e. Q_2) is ready. Obviously, Method-III requires a complicated timing allocation, a sample-and-hold block as well as faster integrators.

4) As shown in Eq. (2. c), Method-IV introduces an error correction technique [10]. It intentionally introduces a unit delay (i.e. z^{-1}) for the delay-free path such that this path can be implemented. With a such delay, an error is induced in the analog domain. Nevertheless, such error is subsequently corrected in the digital domain by introducing an additional term of (1)-z^{-1}). Note that, the error induced in the analog domain will slightly increase the input amplitude of the QTZ. This problem can be alleviated by using a multi-bit QTZ or scaling down the summing coefficients.

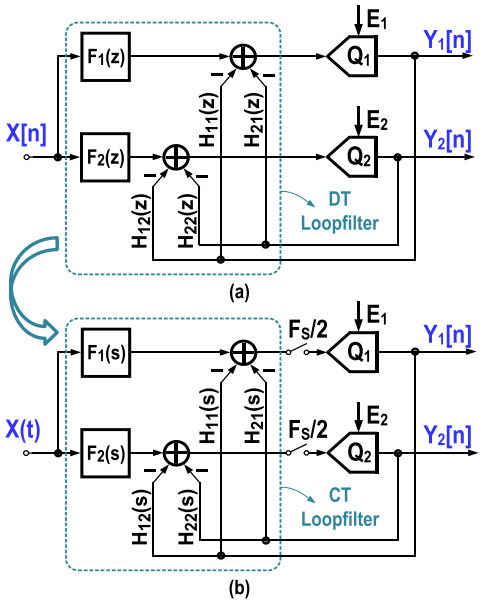

Fig. 2. (a) An equivalent 2x TI DT DSM and (b) an equivalent 2x TI CT DSM.

Overall, Method-I, III and IV all correspond to the analog extrapolation technique without any QN penalty. Method-II has been developed from Method-I based on digital extrapolation. It can significantly simplify the implementation, especially for large interleaving factor (i.e. 4x). But a large SQNR loss is inevitable. As for the methods based on analog extrapolation, the differences are the following. The drawback of Method-I is that the input signal amplitude of the QTZ (located in the extrapolated channel) becomes extremely large without injecting the feedback of Y_2. Method-III poses stringent design requirements for circuitry modules. In contrast, Method-IV implements the delay-free feedback path with affordable hardware overhead. Hence, we choose Method-IV to implement the target 2x TI CT DSM.

C. DT-to-CT Conversion

To implement DT-to-CT conversions, first, we need to recognize the existing loop filters of the TI DT DSM [14]. Fig. 2 (a) shows an equivalent simplified 2x TI DT DSM. As observed, there exist six loop filters, namely, $F_1(z)$, $F_2(z)$, $H_{11}(z)$, $H_{12}(z)$, $H_{21}(z)$ and $H_{22}(z)$. Note that $F_i(z)$ means the transfer function from the input signal to the QTZ input in the i^{th} channel, and $H_{jk}(z)$ means the loop filter from the output of j^{th} QTZ to the k^{th} QTZ input. Next, we can convert the DT loop filters into their equivalent CT loop filters (cf. Fig. 2(b)) by using the classical impulse invariant transformation. Therefore, an equivalent 2x TI CT DSM can be constructed while its STF can be analyzed, which would be shown in Section III-B.

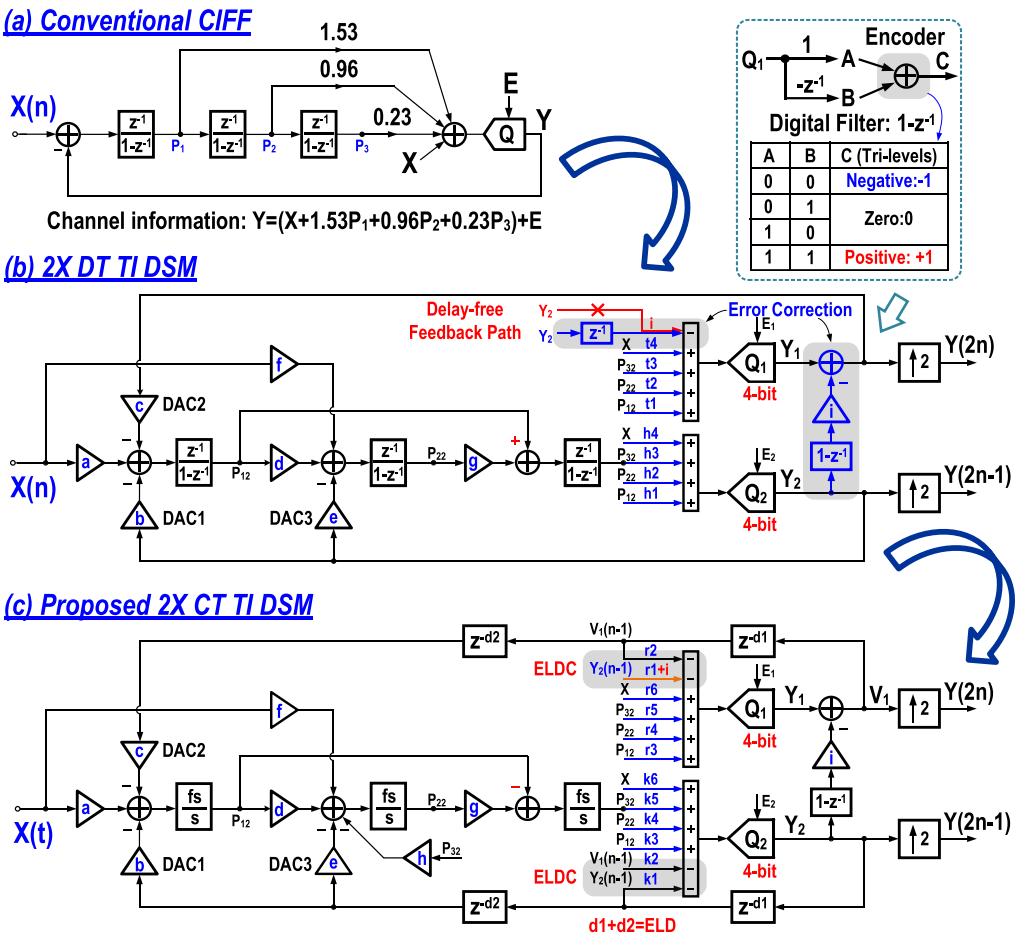

Fig. 3. (a) A 3rd-order CIFF single-channel DT DSM (b) an equivalent 2x TI 3rd-order CIFF DT DSM (c) an equivalent 2x TI 3rd-order CIFF CT DSM.

III. Proposed Two-Channel TI 3rd-Order CT DSM

A. Derivation of 2x TI CT DSM

Fig. 3(a) shows a general 3rd-order DT DSM, where a CIFF loop filter is employed with an input feedforward path. With selecting the maximum out-of-band gain as 2.25, the target NTF is given by,

$$NTF = \frac{(1-z^{-1})^3}{1-1.467z^{-1}+0.8917z^{-2}-0.1967z^{-3}} \quad (4)$$

As shown in Fig. 3(a), the expression of each node (i.e. each integrator output and the final output) during the $(2n)^{\text{th}}$ time slot can be obtained as follows,

$$\begin{aligned} P_1(2n) &= P_1(2n-1) + X(2n-1) - Y(2n-1) \\ P_2(2n) &= P_1(2n-1) + P_2(2n-1) \\ P_3(2n) &= P_2(2n-1) + P_3(2n-1) \\ Y(2n) &= Q[X(2n) + 1.53P_1(2n) + 0.96P_2(2n) \\ &\quad + 0.23P_3(2n)] \end{aligned} \quad (5)$$

Furthermore, based on the recursive operations, we can derive the corresponding expressions of each node for the subsequent $(2n+1)^{\text{th}}$ time slot. To facilitate the following derivations, we define the representation symbols for each node of different channels as follows,

$$X_1(n) = X(2n),\ X_2(n) = X(2n-1) \quad (6)$$

$$P_{11}(n) = P_1(2n),\ P_{12}(n) = P_1(2n-1) \quad (7)$$

$$P_{21}(n) = P_2(2n),\ P_{22}(n) = P_2(2n-1) \quad (8)$$

$$P_{31}(n) = P_3(2n),\ P_{32}(n) = P_3(2n-1) \quad (9)$$

$$Y_1(n) = Y(2n),\ Y_2(n) = Y(2n-1) \quad (10)$$

Note that, for $P_{ij}(n)$, i refers to the i^{th} integrator output and j refers to the j^{th} channel. On the other hand, due to the oversampling property, it can be supposed that $X_1(n) = X_2(n)$ and then we uniformly define them as $X(n)$ [9]. By combining all nodes' expressions during $(2n)^{\text{th}}$ and $(2n+1)^{\text{th}}$ time slots, we can obtain the final expressions in z-domain for the integrators' outputs of the known channel as well as the outputs of both QTZs (detailed derivations are given in the Appendix):

$$P_{12}(z) = \frac{z^{-1}}{1-z^{-1}}(2X(z) - Y_1(z) - Y_2(z)) \quad (11)$$

$$P_{22}(z) = \frac{z^{-1}}{1-z^{-1}}(X(z) + 2P_{12}(z) - Y_2(z)) \quad (12)$$

$$P_{32}(z) = \frac{z^{-1}}{1-z^{-1}}(P_{12}(z) + 2P_{22}(z)) \quad (13)$$

$$\begin{aligned} Y_1(z) &= Q[2.53X(z) + 2.49P_{12}(z) \\ &\quad + 1.19P_{22}(z) + 0.23P_{32}(z) - 1.53Y_2(z)] \end{aligned} \quad (14)$$

$$\begin{aligned} Y_2(z) &= Q[X(z) + 1.53P_{12}(z) \\ &\quad + 0.96P_{22}(z) + 0.23P_{32}(z)] \end{aligned} \quad (15)$$

Based on Eq. (11)-(15), we can construct the extrapolating 2x TI DT DSM, which is illustrated in Fig. 3(b). Note that the issue regarding the delay-free feedback path arises from Eq. (14), where the input of the 1st QTZ (i.e. Q_1) is directly linked to $Y_2(n)$. Using the aforementioned Method-III, we can eliminate the delay-free feedback path by replacing $Q[Y_2(n)]$ with $Q[Y_2(n\text{-}1)]\text{-}Y_2(n-1)+Y_2(n)$. Such a method would not affect the NTF of the TI DSM while the input amplitude of the 1st QTZ will be slightly increased due to the delayed feedback signal.

Next, we will present the DT-to-CT conversions to construct the final proposed 2x TI CT DSM. First, as observed in Fig. 3(b), we could recognize the corresponding six loop filters ($F_1(z)$, $F_2(z)$, $H_{11}(z)$, $H_{12}(z)$, $H_{21}(z)$ and $H_{22}(z)$, c.f. Fig. 2), respectively. Considering the ELD time of 0.5Ts, by using the impulse-invariant transformation, we could obtain the according CT loop filters regarding the feedback signal (i.e. Y_1 and Y_2), as shown in the below matrix,

$$\begin{bmatrix} H_{11}(s) \\ H_{12}(s) \\ H_{21}(s) \\ H_{22}(s) \end{bmatrix} = \begin{bmatrix} 0.91 & 2.14 & 2.45 & 0.98 \\ 0.91 & 1.69 & 1.49 & 0.56 \\ 0.91 & 2.60 & 3.64 & 1.51 \\ 0.91 & 2.14 & 2.45 & 0.98 \end{bmatrix} \begin{bmatrix} 1/s^3 \\ 1/s^2 \\ 1/s \\ 1 \end{bmatrix} \tag{16}$$

Note that the ELD compensation (ELDC) requires the zeroth-order DAC feedback paths to restore the NTF. Therefore, the gains (i.e. r_6 and k_6 in both channels) of the input feedforward paths need to be increased to cater to the introduced zeroth-order DAC feedback such that the output swings of both adders could be minimized. Then, the signal-related loop filters $F_{1,2}(s)$ could be eventually determined as follows,

$$\begin{bmatrix} F_1(s) \\ F_2(s) \end{bmatrix} = \begin{bmatrix} 1.83 & 4.75 & 6.09 & 5.02 \\ 1.83 & 3.83 & 3.95 & 2.53 \end{bmatrix} \begin{bmatrix} 1/s^3 \\ 1/s^2 \\ 1/s \\ 1 \end{bmatrix} \tag{17}$$

To simplify the circuitry implementation, for the 1st channel, as shown in Fig. 3(c), the ELDC feedback path from $Y_2(n\text{-}1)$ can be merged with the original $Y_2(n\text{-}1)$, resulting in a final feedback gain of (r_1+i). Note that, as depicted in Fig. 3(c), there exists one extra DAC3 feedback in the 2x TI CIFF-based architecture, which contradicts the so-called CIFF topology. Indeed, such extra feedback DAC3 comes from the TI extrapolation process. Practically, Y_2 signal is required to obtain the output (i.e. P_{22}) of the second integrator. More details can be found in Appendix (cf. Eq. (49)). Theoretically, based on a CIFF architecture, such Y_2 signal can be obtained by reusing the outermost DAC (i.e. DAC1). However, owing to the TI extrapolation technique, the node information of the known CIFF-based channel needs to be used to predict the output of the other channel. Hence, we add another extra Y_2 feedback path (i.e. DAC3) to make the solutions of all variables flexible. Despite the extra DAC3, the TI CIFF-based architecture can still preserve the benefits of the CIFF topology, such as small swing at internal nodes (i.e. the outputs of the 1st and 2nd integrators).

B. STF Analysis

To analyze the signal transfer function (STF) of the 2x TI CT DSM, we firstly need to obtain the NTF of its original DT counterpart. Overall, after the multiplexing, we could express the final output as the following two formats,

$$Y(z) = Y_1(z^2)z^{-1} + Y_2(z^2) \tag{18}$$

$$Y(z) = STF(z)X(z) + NTF_1(z)E_1(z) + NTF_2(z)E_2(z) \tag{19}$$

Note that the z^2 term shows the effect of the up-samplers in the final multiplexing block (cf. Fig. 1 middle).

On the other hand, based on Fig. 2(a), we can obtain the following equations,

$$X(z)F_1(z) - Y_1(z)H_{11}(z) - Y_2(z)H_{21}(z) + E_1(z) = Y_1(z) \tag{20}$$

$$X(z)F_2(z) - Y_1(z)H_{12}(z) - Y_2(z)H_{22}(z) + E_2(z) = Y_2(z) \tag{21}$$

By solving Eq. (20)-(21), we can obtain the expressions for $Y_1(z)$ and $Y_2(z)$,

$$Y_1(z) = \frac{\begin{vmatrix} X(z)F_1(z) + E_1(z) & H_{21}(z) \\ X(z)F_2(z) + E_2(z) & 1 + H_{22}(z) \end{vmatrix}}{\begin{vmatrix} 1 + H_{11}(z) & H_{21}(z) \\ H_{12}(z) & 1 + H_{22}(z) \end{vmatrix}} \tag{22}$$

$$Y_2(z) = \frac{\begin{vmatrix} 1 + H_{11}(z) & X(z)F_1(z) + E_1(z) \\ H_{12}(z) & X(z)F_2(z) + E_2(z) \end{vmatrix}}{\begin{vmatrix} 1 + H_{11}(z) & H_{21}(z) \\ H_{12}(z) & 1 + H_{22}(z) \end{vmatrix}} \tag{23}$$

By substituting $Y_1(z)$ and $Y_2(z)$ into Eq. (18) and comparing it to Eq. (19), we could recognize the final NTF_1 and NTF_2 for E_1 and E_2 as follows,

$$NTF_1(z) = \frac{\left[1 + H_{22}\left(z^2\right)\right]z^{-1} - H_{12}\left(z^2\right)}{\left[1 + H_{11}\left(z^2\right)\right]\left[1 + H_{22}\left(z^2\right)\right] - H_{21}\left(z^2\right)H_{12}\left(z^2\right)} \tag{24}$$

$$NTF_2(z) = \frac{\left[1 + H_{11}\left(z^2\right)\right] - H_{21}\left(z^2\right)z^{-1}}{\left[1 + H_{11}\left(z^2\right)\right]\left[1 + H_{22}\left(z^2\right)\right] - H_{21}\left(z^2\right)H_{12}\left(z^2\right)} \tag{25}$$

Then, we could express the STF of the 2x TI CT DSM as,

$$STF(w) = NTF_1\left(e^{jwTs}\right)F_1(jw) + NTF_2\left(e^{jwTs}\right)F_2(jw) \tag{26}$$

Based on Eq. (17) and Eq. (24)-(26), Fig. 4 plots the STF of the 2x TI CT DSM. As observed, owing to the employment of CIFF architecture, there exists a foreseen STF peaking. Furthermore, the STF peaking becomes higher with the presence of the ELD and its compensation. Such peaking may be problematic with the presence of out-of-band blockers in wireless communication applications. The DSM will saturate if large amplitude of out-of-band blockers exist. Nevertheless, this work can distribute input paths to maximumly flatten the STF around the peaking [5]. By introducing additional input

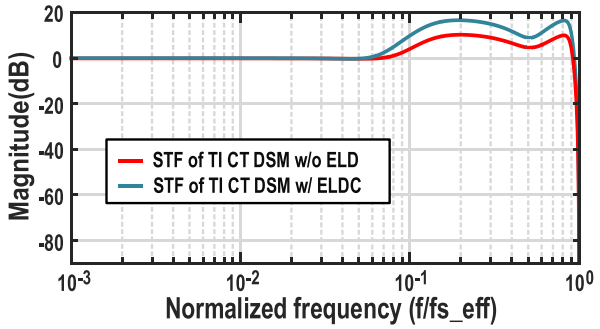

Fig. 4. The STFs of the 2x TI CT DSM without ELD and with ELDC.

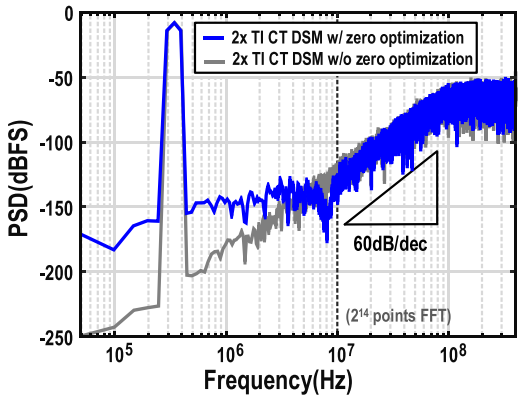

Fig. 5. Simulated output spectrum with and without zero optimization.

branches at the input of the second and third integrators while adjusting coefficients k_6 and r_6 to change $F_1(s)$ and $F_2(s)$, the STF peaking can be significantly suppressed (not shown here for simplicity). Note that the NTF is not affected by this. Furthermore, a simple first-order filter integrated with a trans-impedance amplifier in the receiver signal chain can be used to suppress the remaining STF peaking if necessary [5].

C. Zero Optimization

For a 3rd-order noise-shaping function, using zero optimization can further boost the achievable SQNR by effectively suppressing the QN near the band edge. For a general single-channel DSM, it is feasible to apply zero optimization into various topologies, namely CIFF, cascaded integrators with distributed feedbacks (CIFB) and the mixed CIFF-FB. However, when it comes to the TI system, as depicted in Fig. 3(c), only the CIFF structure allows implementing the zero optimization by adding a local resonator between the 2nd and 3rd integrators. Note that there is no additional DAC injection between those two integrators. The intuitive explanation is the following. Only for the CIFF topology, the function of local resonator feedback could apply to $NTF_1(z)$ and $NTF_2(z)$ together, thus generating a desired notch near the band edge. As shown in Fig. 5, with an equivalent OSR of 40, the achievable SQNR gets augmented by 7dB by using zero optimization. Note that the implementation of zero optimization in the TI DSM is valuable as the usable OSR further decreases.

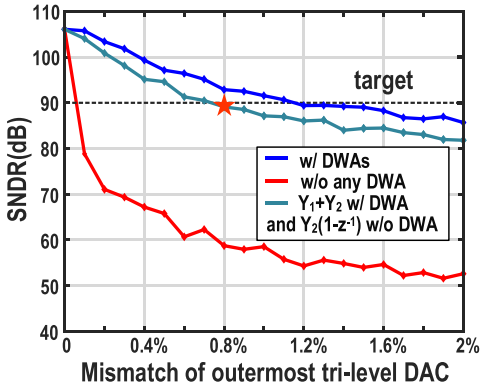

Fig. 6. The achievable SNDR versus the mismatch of outermost tri-level DACs.

D. DAC Mismatch

As shown in Fig. 3(c), there are more DACs involved in the TI DSM, compared to a general single-channel DSM. Thereby, we need to carefully address the DAC nonlinearities to achieve the desired resolution. For outermost DACs, their linearities are way significant. Note that the digital outputs Y_1 and Y_2 from two QTZs can be combined as a tri-level format (cf. Fig. 3 top right), thus resulting in a tri-level outermost DAC [5]. Before the tri-level encoder, the data weighting averaging (DWA) blocks are applied for Y_1 and Y_2, respectively. Moreover, by using the error correction technique to eliminate the delay-free feedback path, $Y_2(1)-z^{-1})$ needs to be generated and further given back into the loop. Similarly, we use tri-level DAC to implement $Y_2(1)-z^{-1})$, thus reducing the DAC unit cells. Note that the high-pass filtering of (1)-z^{-1}) could inherently suppress the signal component, thus significantly improving the tolerance to this DAC nonlinearity.

Fig. 6 shows the performance of the outermost DACs with and without using DWAs over various DAC mismatch. As we expect, the tri-level DAC formed by Y_1 and Y_2 requires the DWA module, while the mismatch of the tri-level DAC formed by $Y_2(1)-z^{-1})$ will affect the performance slightly without using DWA. To achieve the target SNDR of 90dB, it is necessary to keep the static mismatch of the outermost DACs within 0.8%. Note that the current steering topology is selected for the outermost DAC, which could ensure such value with proper size and careful layout floorplan in the modern CMOS process.

In summary, the benefits of the proposed CT DSM are: 1) increase an effective OSR by 2x; 2) it allows to implement zero optimization into TI DSM, thus further boosting the performance; 3) it reduces the number of required feedback DACs as large as 5, compared to CIFB topology; 4) DWA could be potentially available to address the nonlinearity of the outermost DACs as the practical clock rate is reduced by 2x.

IV. Circuit Implementation

Fig. 7 shows circuitry-level block diagram of the proposed 2x TI CT DSM, where 4b QTZs are used for both channels. It employs a 3rd-order CIFF loop filter with internal feed-forward paths and input signal feedforward paths. For the

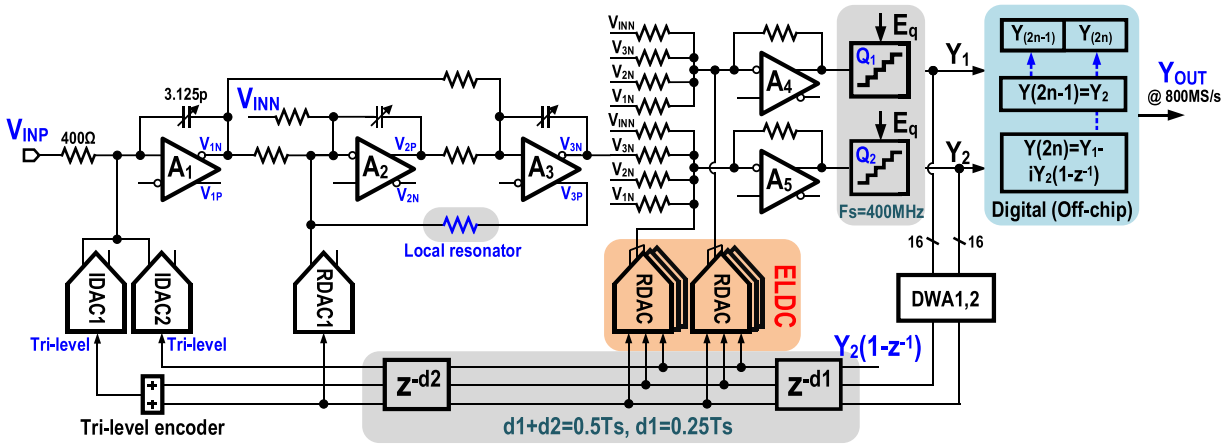

Fig. 7. Simplified single-ended schematic of the proposed 2x TI 3rd-order CIFF-based CT DSM.

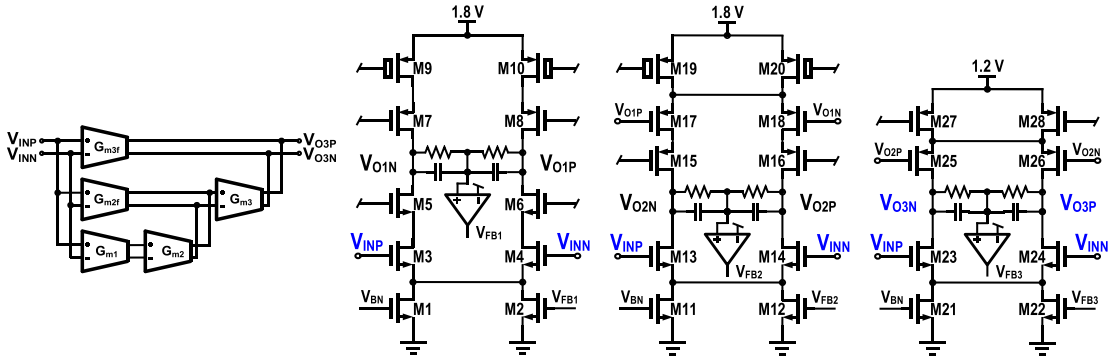

Fig. 8. Schematic of a three-stage operational amplifier with feedforward compensation.

three main DACs, non-return-to-zero (NRZ) current steering DACs (IDAC1 and IDAC2) are employed for the outermost DACs while resistive DAC (RDAC1) is used for the inner DAC. As for the innermost DAC feedbacks, all employ the topology of RDAC. As aforementioned, the feedback signal of $Y_2(1) - z^{-1}$) can be implemented by a tri-level encoder plus a tri-level DAC. Considering the thermal noise limit, we set the input resistance to be 400ohm for the 1st integrator. To compensate for the maximal ±40% process spread of the RC time constants, all capacitors in the loop filter are implemented as binary capacitor banks consisting of a fixed part and a programmable part (5b for 1st integrator, 4b for 2nd and 3rd ones). For the feedforward adders, we choose a resistor-based summing operational amplifier (op-amp) to sum up the input signal, the outputs of three integrators, and the feedback DACs used for ELDC. Note that a passive summer is not used here owing to the concern of large gain attenuation [15], [16], [17]. To reduce the output swing of the adders, we apply a scaled-down gain of 1/4 for both adders. Accordingly, the references of the QTZs are scaled down by the same factor to restore the NTF, resulting in a less equivalent LSB of the QTZ [18]. Hence, it poses a higher requirement for the offset of the comparator.

A. Feedforward Amplifiers

In the proposed DSM, we choose a three-stage op-amp architecture with feedforward compensation [19] for all integrators and adders. Compared with miller-compensated op-amps, feedforward op-amps are more favored in CT DSMs. It is because they can achieve a higher gain at the band edge with less power by reusing the bias current [20], [21], [22], [23], [24]. Fig. 8 shows detailed schematic of the three-stage feedforward op-amp. The 1st and 2nd stages use telescopic architecture, which acts as the input stage G_{m1} and the second stage G_{m2}. As for the 3rd output stage (G_{m3}), a complementary differential topology is employed without using cascode. Transistors M13−M14 and M23-M24 implement the input feedforward paths (G_{m2f} and G_{m3f}), respectively. Note that 1.8V supply is used for the 1st and 2nd stages while 1.2V supply is employed for the last stage. For each stage, we use an active common-mode feedback (CMFB) amplifier to stabilize the output common-mode (CM) voltage. Note that 900mV is set as the CM voltage of the 1st stage while 600mV is set for the CM voltage of the last two stages.

The 1st integrator consumes a DC current of 2.3 mA from the 1.8 V supply and 1.3 mA from the 1.2 V supply. Moreover, the three CMFB amplifiers, consume an additional DC current of 0.9mA altogether. With cascading three stages, the op-amp1 can achieve an open-loop DC gain of over 60dB. When considering the closed-loop AC response, the op-amp1 provides an in-band gain of over 33dB and a unity gain frequency (UGF) greater than 1.6GHz. The loop UGFs of op-amp2 (the 2nd integrator), op-amp3 (the 3rd integrator), op-amp4 (the 1st adder, c.f. Fig. 7) and op-amp5 (the 2nd adder, c.f. Fig. 7) are

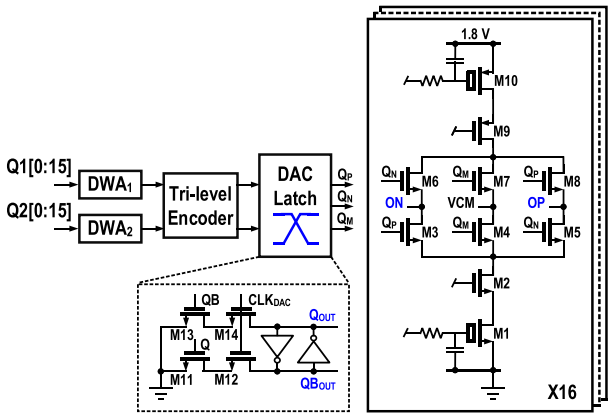

Fig. 9. Schematic of one complementary IDAC unit cell.

1.47GHz, 1.21GHz, 576MHz and 733MHz, respectively. Note that we use the same op-amp for the last four op-amps due to the limited design time. Each one consumes 3.1mW power, which can be potentially reduced with a customized design.

B. IDAC Unit Cell

Fig. 9 shows the complementary IDAC unit cell used for the outermost DAC. Compared to a traditional differential IDAC, the complementary topology only requires half of the bias current for a given differential LSB. As shown, each DAC unit cell consists of the current source transistor M1 and M10, the cascode transistors M2 and M9, the switch transistors M3∼M8 as well as the DAC latch. With supply at 1.8V, M1 and M10, whose drain is biased at 1.05V and 0.6V respectively, provide large voltage headroom for low noise performance and better matching. In addition, passive low-pass filters are used to further suppress the thermal noise contribution from the biasing circuit [25]. The DAC latch contains the transistors M11∼M14 and uses cross-coupled inverters to generate high-crossing switching [26], thus reducing the dynamic glitches. The standard deviation of the outermost IDAC unit current mismatch is ∼0.5%. With using the DWAs, the simulated mean THD is ∼94dB, which could satisfy the target requirement.

C. Quantizer

Fig. 10 depicts the dynamic comparator schematic used in the 4b flash QTZ [27]. The dynamic comparator consists of two parts: the clock-enabled pre-amplifier and the regenerative latch. The nodes DP and DN are reset to VDD in the negative phase of CLK. When CLK is high, DP and DN are discharged to the ground. The rate of discharge is determined by the input signal pair (VINP and VINN) and the reference pair (VREFP and VREFN). If DN falls faster than DP, RN will be latched to the ground while RP will be latched to VDD, and vice versa. Besides, a pair of transistors, with half the size of the input transistor, is connected at the input to minimize the kickback noise with a slightly delayed clock (not shown here for simplicity) [24].

We use a foreground calibration to reduce the offset of each comparator, where the nominal value is ∼20mV before

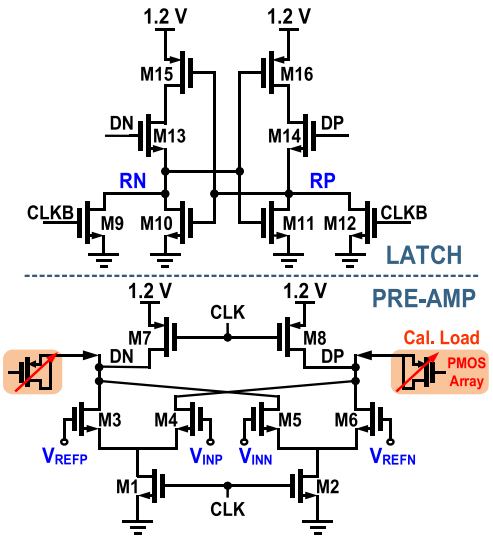

Fig. 10. Schematic of a comparator unit cell.

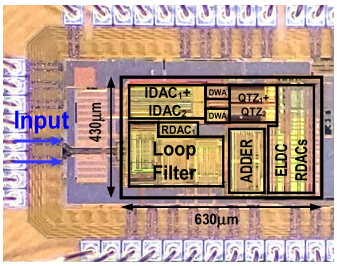

Fig. 11. The prototype chip micrograph.

the calibration. Note that the PMOS-based capacitor array is connected to DP and DN with 5b trimming code. After the calibration, the offset can be achieved less than ∼5mV, which is ∼LSB/8 (LSB=37.5mV). Hence, the effect of the offset can be negligible to the resolution of the QTZ.

V. Experimental Results

The prototype of the proposed 2x TI CT DSM is fabricated in 65nm CMOS process. Fig. 11 shows the chip micrograph, where the active core area is 0.27 mm^2.

Fig. 12 shows the measured FFT output spectrum by applying a −3.3dBFS input at 1.8MHz. Note that each DSM channel operates at 400MHz while the final equivalent sampling rate is 800MHz. As desired, there exists a 60dB/dec slope in the output spectrum. The measured SNDR/SNR/SFDR improves from 59.3dB/65.2dB/60.6dB (both DWAs off) to 74.6dB/75.1dB/86.7dB (outmost and internal DWA both on) over a 10MHz BW. Furthermore, by activating the DWAs for the outermost DACs and deactivating the DWAs for all inner DACs, we could obtain the best measured SNDR/SNR/SFDR of 75.5dB/75.8dB/89.7dB.

Fig. 13 depicts a two-tone measurement result. With two inputs of -9.5dBFS at 9MHz and 9.4MHz, the third intermodulation distortions (IMD3) are 80dBc and 78dBc, respectively. Fig. 14 plots the SNR/SNDR over the input signal power, where the DR is measured to be 79dB. Fig. 15 illustrates the measured STF, which is almost in line with the simulated STF.

TABLE I
PERFORMANCE SUMMARY AND BENCHMARK WITH STATE-OF-THE-ART DSMS

	This Work	[13] JSSC'06	[9] JSSC'21	[8] JSSC'20	[30] JSSC'22	[31] TCAS-I'20	[29] TCAS-I'19
Architecture	**TI 2x CT-DSM**	TI 2x CT-DSM	TI 4x DT-DSM	TI 4x NS-SAR	CT DSM	CT DSM	CT DSM
Process (nm)	**65**	180	28	40	65	40	28
Supply (V)	**1.2/1.8**	1.8	1/1.15/1.5	1	1.1/1.5	1.1/1.8	-
BW(MHz)	**10**	10	5	50	18.75	75	85
F_S (MHz)	**In/Out =400/800**	In/Out =100/200	In/Out =520/2080	In/Out =100/400	600	2400	1700
SNDR (dB)	**75.5**	57.2	86.1	70.4	73.4	67.3	68.5
SNR (dB)	**75.8**	58.4	N/A	N/A	74.5	68.1	71.1
DR (dB)	**79**	60.8	90	71.7	78.3	70	72.7
Power (mW)	**33.73**	101	23.1	13.0	17.85	27	23.9
Area (mm^2)	**0.27**	1	0.07	0.06	0.18	0.675	0.12
FoM_{SNDR} (dB)	**160.2**	137.2	169.5	166.3	163.6	161.7	164
FoM_{DR} (dB)	**163.7**	140.8	173.4	167.6	168.5	164.4	168.2

$$FoM_{SNDR} = SNDR + 10 \cdot \lg(\frac{BW}{Power}) \quad FoM_{DR} = DR + 10 \cdot \lg(\frac{BW}{Power})$$

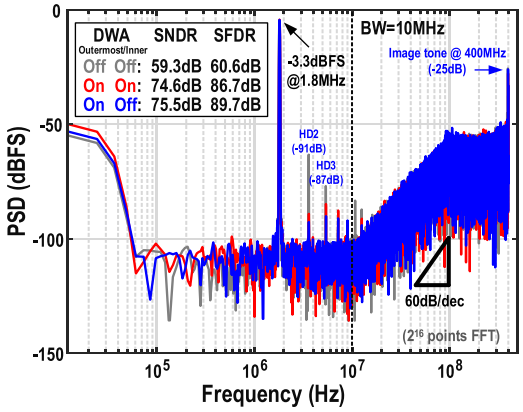

Fig. 12. Measured FFT output spectrum of the prototype DSM.

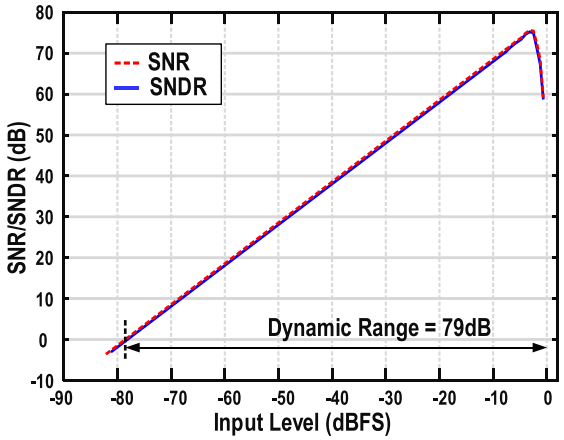

Fig. 14. Measured SNR/SNDR versus input signal power.

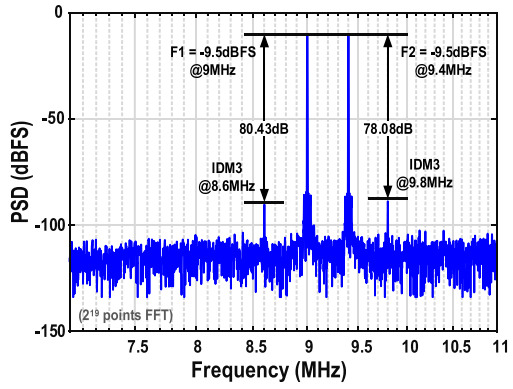

Fig. 13. Measured FFT spectrum of the IMD_3.

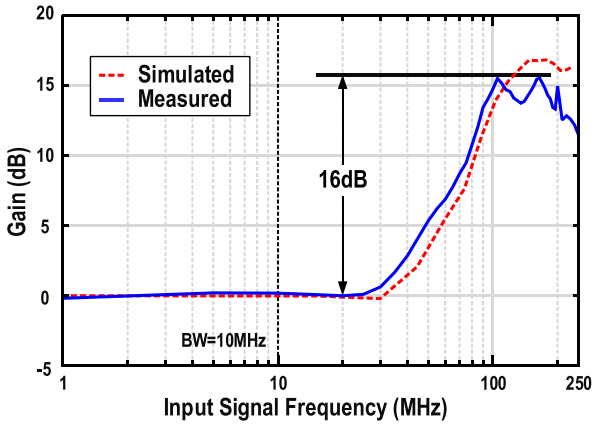

Fig. 15. Measured STF versus simulated STF.

It is found that a peaking as high as 16dB exists at ~150MHz. As aforementioned, some extra feed-in paths can be introduced to suppress the peaking in the STF [5], [28].

Fig. 16 shows the power breakdown, where the total power consumption is 33.73mW at 1.2 and 1.8 V supplies. Note that

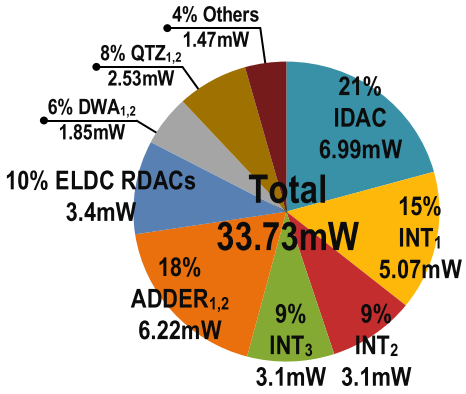

Fig. 16. Power breakdown of the prototype modulator.

1.8V is used for the IDACs and all op-amps while 1.2V is used for other blocks. To achieve a low thermal noise, the input resistance is chosen as 400ohm, resulting in the power consumption of IDACs of 6.99mW. It contributes 21% of total power, which could be further reduced with a higher input resistance. Moreover, owing to the limited design time, we use the same op-amp for the 2nd and 3rd integrator as well as two adders. Their power consumption can be further potentially reduced with optimized design. Table I summarizes the performance of this prototype while making a comparison to state-of-the-art TI DSMs as well as general single-channel DSMs [8], [9], [13], [29], [30], [31]. This work exhibits a Schreier Figure of Merit (FoM) of 163.7dB based on DR.

VI. Conclusion

This paper presents a 2x TI CT 3rd-order DSM based on CIFF architecture. The whole 2x TI DSM is constructed based on one complete channel using extrapolation. The CIFF architecture could significantly reduce the number of required DACs while making zero optimization feasible for the TI DSM. Note that, two active adders are required to support the summation of multiple inputs. Fabricated in 65nm CMOS, the proposed DSM achieved an equivalent output rate of 800MS/s, while the analog channel only operates at 400MHz. The prototype achieves SNDR/SNR/DR of 75.5dB/75.8dB/79dB over a 10MHz BW. It dissipates 33.73mW power, yielding a Schreier FoM of 163.7dB based on DR.

Appendix

Here we present detailed mathematical derivations to construct an extrapolating TI CT DSM. As shown in Fig. 3(a), the expression of each node (i.e. the integrator output and the final output) during the $(2n)^{\text{th}}$ time slot can be obtained as follows,

$$P_1(2n) = P_1(2n-1) + X(2n-1) - Y(2n-1) \quad (27)$$
$$P_2(2n) = P_1(2n-1) + P_2(2n-1) \quad (28)$$
$$P_3(2n) = P_2(2n-1) + P_3(2n-1) \quad (29)$$
$$Y(2n) = Q[X(2n) + 1.53P_1(2n) + 0.96P_2(2n) + 0.23P_3(2n)] \quad (30)$$

Similarly, the above output expressions are iterated for the subsequent $(2n+1)^{\text{th}}$ time slot,

$$P_1(2n+1) = P_1(2n) + X(2n) - Y(2n) \quad (31)$$
$$P_2(2n+1) = P_1(2n) + P_2(2n) \quad (32)$$
$$P_3(2n+1) = P_2(2n) + P_3(2n) \quad (33)$$
$$Y(2n+1) = Q[X(2n+1) + 1.53P_1(2n+1) + 0.96P_2(2n+1) + 0.23P_3(2n+1)] \quad (34)$$

To facilitate the following derivations, we rewrite the representation symbols for each node of different channels as follows,

$$X_1(n) = X(2n),\ X_2(n) = X(2n-1) \quad (35)$$
$$P_{11}(n) = P_1(2n),\ P_{12}(n) = P_1(2n-1) \quad (36)$$
$$P_{21}(n) = P_2(2n),\ P_{22}(n) = P_2(2n-1) \quad (37)$$
$$P_{31}(n) = P_3(2n),\ P_{32}(n) = P_3(2n-1) \quad (38)$$
$$Y_1(n) = Y(2n),\ Y_2(n) = Y(2n-1) \quad (39)$$

Note that, for $P_{ij}(n)$, i refers to the i^{th} integrator output and j refers to the j^{th} channel. On the other hand, due to the oversampling property, it can be supposed that $X_1(n) = X_2(n)$ and then we uniformly define them as $X(n)$ [9].

Based on Eq. (35)-(39), we could rewrite Eq. (27)-(30) as,

$$P_{11}(n) = P_{12}(n) + X(n) - Y_2(n) \quad (40)$$
$$P_{21}(n) = P_{12}(n) + P_{22}(n) \quad (41)$$
$$P_{31}(n) = P_{22}(n) + P_{32}(n) \quad (42)$$
$$Y_1(n) = Q[X(n) + 1.53P_{11}(n) + 0.96P_{21}(n) + 0.23P_{31}(n)] \quad (43)$$

Similarly, Eq. (31)-(34) are rewritten as follows,

$$P_{12}(n+1) = P_{11}(n) + X(n) - Y_1(n) \quad (44)$$
$$P_{22}(n+1) = P_{11}(n) + P_{21}(n) \quad (45)$$
$$P_{32}(n+1) = P_{21}(n) + P_{31}(n) \quad (46)$$
$$Y_2(n) = Q[X(n) + 1.53P_{12}(n) + 0.96P_{22}(n) + 0.23P_{32}(n)] \quad (47)$$

Combining Eq. (40)-(47), the output expression in z-domain for each integrator of the 2nd channel can be given by,

$$P_{12}(z) = \frac{z^{-1}}{1-z^{-1}}(2X(z) - Y_1(z) - Y_2(z)) \quad (48)$$
$$P_{22}(z) = \frac{z^{-1}}{1-z^{-1}}(X(z) + 2P_{12}(z) - Y_2(z)) \quad (49)$$
$$P_{32}(z) = \frac{z^{-1}}{1-z^{-1}}(P_{12}(z) + 2P_{22}(z)) \quad (50)$$

Moreover, the outputs of two channels can be expressed as,

$$Y_1(n) = Q[2.53X(n) + 2.49P_{12}(n) + 1.19P_{22}(n) + 0.23P_{32}(n) - 1.53Y_2(n)] \quad (51)$$
$$Y_2(n) = Q[X(n) + 1.53P_{12}(n) + 0.96P_{22}(n) + 0.23P_{32}(n)] \quad (52)$$

Based on Eq. (48) to (52), a 2x TI DT architecture can be initially constructed, as shown in Fig. 3(b). Furthermore,

we employ the error correction technique to eliminate the delay-free loop by adjusting the expression of $Y_1(n)$ to,

$$\begin{aligned} Y_1(n) = Q\,[&2.53X(n) + 2.49P_{12}(n) + 1.19P_{22}(n) \\ &+0.23P_{32}(n) - 1.53Y_2(n-1)] \\ &- 1.53\,(Y_2(n) - Y_2(n-1)) \end{aligned} \tag{53}$$

Based on Eq. (53), the coefficient of the error correction branch can be obtained.

Next, we consider the DT-to-CT conversions. First, based on Fig. 3(b), the six loop filters (cf. Fig. 2) can be derived as,

$$\begin{bmatrix} F_1(z) \\ F_2(z) \\ H_{11}(z) \\ H_{12}(z) \\ H_{21}(z) \\ H_{22}(z) \end{bmatrix} = \begin{bmatrix} 1.83 & 5.66 & 6.17 & 2.53 \\ 1.83 & 4.75 & 4.02 & 1 \\ 0.91 & 2.60 & 2.49 & 0 \\ 0.91 & 2.14 & 1.53 & 0 \\ 0.91 & 3.06 & 3.68 & 1.53 \\ 0.91 & 2.60 & 2.49 & 0 \end{bmatrix} \begin{bmatrix} \left(\frac{z^{-1}}{1-z^{-1}}\right)^3 \\ \left(\frac{z^{-1}}{1-z^{-1}}\right)^2 \\ \frac{z^{-1}}{1-z^{-1}} \\ 1 \end{bmatrix} \tag{54}$$

By using the impulse-invariant transformations, the corresponding CT loop filters without ELD can be obtained,

$$\begin{bmatrix} F_1(s) \\ F_2(s) \\ H_{11}(s) \\ H_{12}(s) \\ H_{21}(s) \\ H_{22}(s) \end{bmatrix} = \begin{bmatrix} 1.83 & 3.83 & 3.95 & 2.53 \\ 1.83 & 2.92 & 2.26 & 1 \\ 0.91 & 1.69 & 1.50 & 0 \\ 0.91 & 1.23 & 0.77 & 0 \\ 0.91 & 2.14 & 2.45 & 1.53 \\ 0.91 & 1.69 & 1.49 & 0 \end{bmatrix} \begin{bmatrix} \left(\frac{fs}{s}\right)^3 \\ \left(\frac{fs}{s}\right)^2 \\ \frac{fs}{s} \\ 1 \end{bmatrix} \tag{55}$$

When considering the ELD and its compensation, it is very complicated by using manual calculations. Instead, we obtain the coefficients based on the impulse response simulation testbench [32]. Eventually, all the CT loop filters with respect to different orders are listed as follows,

$$\begin{bmatrix} F_1(s) \\ F_2(s) \\ H_{11}(s) \\ H_{12}(s) \\ H_{21}(s) \\ H_{22}(s) \end{bmatrix} = \begin{bmatrix} 1.83 & 4.75 & 6.09 & 5.02 \\ 1.83 & 3.83 & 3.95 & 2.53 \\ 0.91 & 2.14 & 2.45 & 0.98 \\ 0.91 & 1.69 & 1.49 & 0.56 \\ 0.91 & 2.60 & 3.64 & 1.51 \\ 0.91 & 2.14 & 2.45 & 0.98 \end{bmatrix} \begin{bmatrix} 1/s^3 \\ 1/s^2 \\ 1/s \\ 1 \end{bmatrix} \tag{56}$$

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