Weightings in Incremental ADCs: A Tutorial Review

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Abstract – Incremental delta-sigma analog-to-digital converters (IADC) are widely used in modern high-fidelity audio, sensors, and IoT low-power applications. Over the past years, the techniques to implement high-resolution IADCs have been significantly improved, for example, in handling the weighting problems inside the IADCs to overcome thermal noise and DAC mismatch issues. This paper offers a tutorial review on the considerations of weightings in IADCs. The influence of weightings on thermal noise and DAC mismatches is analyzed, and the use of weighting in algorithms is described specifically. The advanced architectures to take advantage of the weightings based on recent academic achievements are presented respectively, with design examples to illustrate the successful practical implementations.

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I. Introduction

In sensor and instrumentation applications, for example, audio, temperature sensing, acceleration and location sensing, and also wearable devices to identify biometrics [1]-[16], the signals to be processed are usually with frequencies from DC to audio bandwidth [1]-[4]. High-resolution analog-to-digital converters (ADC) with a high signal-to-noise ratio (SNR) are in strong demand in these applications. The ADCs in these applications require a high dynamic range because the signal power in most cases is relatively weak. To achieve high resolution in audio bandwidth, while the flicker noise can be suppressed by the use of a chopper [14]-[23], the ADC needs to overcome thermal noise as well [1]-[6]. Moreover, multi-channel sensors need to digitize the input individually with low latency and to be multiplexed easily [1]-[4], [12], [15].

The oversampling technique is one of the best choices for high-resolution ADC design, and as an effective structure, delta-sigma (ΔΣ) ADCs are widely considered [19]-[25]. Fig. 1 (a) shows an example block diagram of the continuously free-running ΔΣ ADC, in which the digital decimator is rather complicated, and the latency of the ΔΣ modulator can be long [2]-[4]. Also, in Fig. 1 (a), the latency from the input to the output is order-dependent. Supposing the input signal was switched to another channel, in that case, the digital filter needs (L+1)OSR (i.e., OSR is short for the over-sampling ratio) clock cycles to settle and then provide the estimation of the input signal of the new channel. Eventually, the traditional free-running ΔΣ modulator architecture was not applicable to multi-channel signal acquisition [1]-[4], [15].

To overcome the long latency of continuously free-running ΔΣ ADC, the incremental ΔΣ ADC can be an alternative [1]-[4]. As shown in Fig. 1 (b), the block diagram is very similar to its free-running counterpart [2], which also consists of an analog modulator and a digital decimator. Unlike the traditional ΔΣ ADC, the IADC clears the memory periodically by resetting the analog modulator and the digital filter, inducing an independent sample-by-sample operation.

For IADCs, the resetting operation breaks the loop's continuity. The digital output codes depend only on the input samples lying within the conversion interval. Thus, it provides a Nyquist-like property [2], [4], [5]. Therefore, the IADC is suitable for multi-channel applications since the digitalization of the input signal is ready at the end of one conversion. Furthermore, the IADC does not suffer from idle tones [1], [2] thanks to its resetting operation, because the pattern signal can be regarded as an offset and can be removed in the digital domain, making the IADC an excellent candidate for the high-performance audio system.

Compared to the ΔΣ modulators, IADCs have unique signal processing characteristics. Specifically, the signal transfer function (STF) of the free-running ΔΣ modulator is usually able to be set as unity (or with some delays), which means that the relative importance (i.e., weights) of all the input samples are equal. Thus the OSR can work well to suppress the thermal noise [2], [5]. Also the DAC mismatches can be effectively suppressed using a general data-weighted averaging (DWA) algorithm [26]-[29]. However, the case in the IADC is different. Due to the resetting operation, the IADC posts equivalently a specific "deadline" to force a finite number of oversampling samples to represent a certain Nyquist output, and the STF is usually not unity. This imposes weighting issues, especially in high-order IADCs, and compromises the effectiveness of the OSR to suppress the thermal noise and DAC mismatches through DWA [30], [31]. Although the effect of non-uniform weighting is disadvantageous for high-order IADCs, some unique designs may make use of this special property and create excellent architectural algorithms to mitigate the problems [30]-[38].

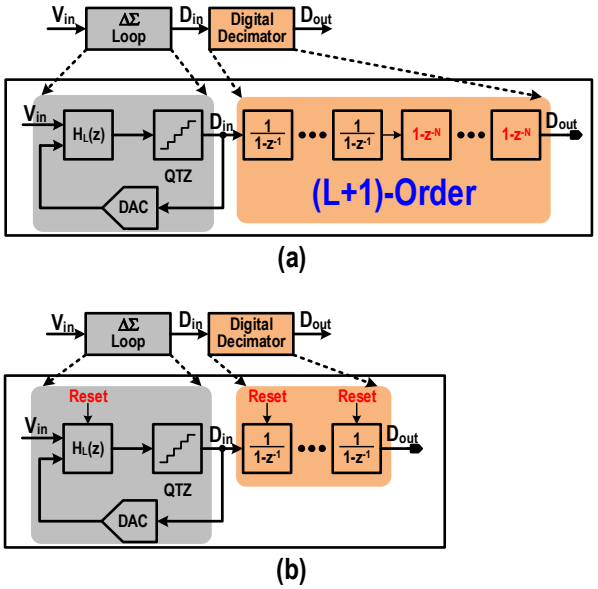

Fig. 1. The block diagram of (a) a ΔΣ ADC in continuously free-running mode and (b) an incremental ADC with reset.

This paper is organized as follows. Section II describes the fundamental theories of IADC. Section III analyzes the influence of weightings on the performance of the IADC. Section IV introduces algorithms based on exponential IADC. The design examples based on weighting in advanced architectures are discussed in Section V. Section VI gives a conclusion to this paper.

II. A Simple Review of IADC Algorithms

a) First-Order IADCs

First presented by Van De Plassche in 1978 in [39], as illustrated in Fig. 2, the IADC is like a ΔΣ ADC with a resetting button. It is easier to observe an IADC in the time domain [6]. At the beginning of each conversion, the integrator, as well as the digital decimator, are reset to clear the previous memory. Then the integrator accumulates the difference between the input signal V_{in} and the signal from feedback DAC $D_k \cdot V_{ref}$. Assume V_{res} is the residue output voltage of the integrator. After N^{th} clock cycles, V_{res} is calculated as:

$$V_{res}[N] = \sum_{i=i}^{N} V_{in}(i) - \sum_{i=i}^{N} D_k(i)\, V_{ref} \tag{1}$$

where $D_k(i)$ represents the digital output codes at i^{th} clock cycle, and N=OSR is the number of clocks per conversion or the oversampling ratio in the IADC. The estimated input signal can be derived as:

$$\overline{V_{in}} = \frac{\sum_{i=1}^{N} D_k(i) V_{ref}}{N} + \frac{V_{res}[N]}{N} \tag{2}$$

The first term of the right-hand side is the digital estimation of V_{in}, which can be regarded as a weighted average of digital output codes. The second term is the quantization error, determined by the residue output voltage of integrator $V_{res(N)}$.

The resolution of the first-order IADC can be derived as:

$$R_{1st} = log_2(N) \tag{3}$$

It can be concluded that for a first-order incremental architecture, the required clock cycle is 2^n for an n-bit resolution, which accumulates the input signal with low efficiency.

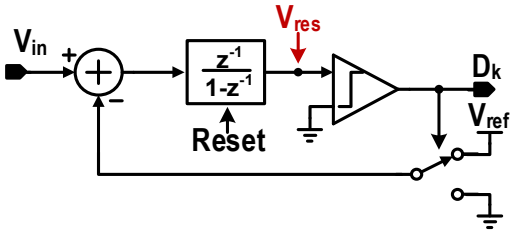

Fig. 2. The block diagram of a first-order IADC.

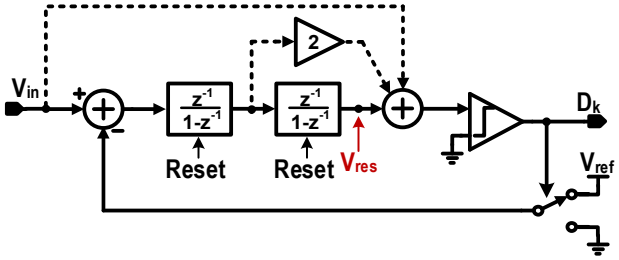

Fig. 3. The block diagram of a second-order IADC.

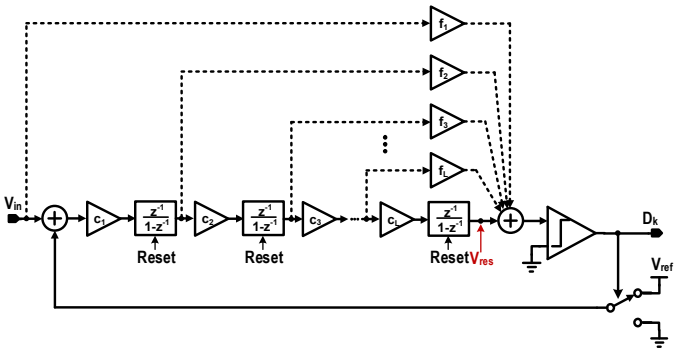

Fig. 4. The block diagram of an L[th]-order IADC.

b) Second-Order IADCs

Cascading integrators can increase the speed of accumulation [2], [5], and the number of clock cycles reduces sharply.

Fig. 3 shows a cascaded-integrator feedforward (CIFF) structure of a second-order IADC with a single-bit quantizer. Using the same model as described earlier in first-order IADC, the estimated input signal for the second-order modulator is calculated as:

$$\overline{V_{in}} = \frac{\sum_{i=1}^{N}\sum_{j=1}^{i-1} D_k(i)V_{ref}}{M} + \frac{V_{res}[N]}{M} \quad (4)$$

where M is the total gain of signal accumulation which is $(N(N+1))/2$.

The resolution of the second-order IADC can be calculated as:

$$R_{2nd} = log_2\left[\frac{N(N+1)}{2}\right] \quad (5)$$

Compared to the first-order, the second-order structure is much more efficient for its faster accumulation and lower power consumption. To achieve a 20-bit resolution, the first-order needs 1048576 clock cycles, while only 1449 clock cycles are required in the second-order structure.

c) High-Order IADCs

Since a second-order IADC is more efficient than a first-order one, high-order IADCs are considered straightforwardly. An L[th]-order single-loop IADC with feedforward paths and a single-bit quantizer is illustrated in Fig. 4.

Based on the accumulation structure above, the input signal can be estimated as:

$$\overline{V_{in}} = \frac{c_1c_2\cdots c_L\sum_{i_1=1}^{N}\sum_{i_2=1}^{i_1-1}\cdots\sum_{i_L=1}^{i_{L-1}-1} D_k(i_L)V_{ref}}{M} + \frac{V_{res}(N)}{M} \quad (6)$$

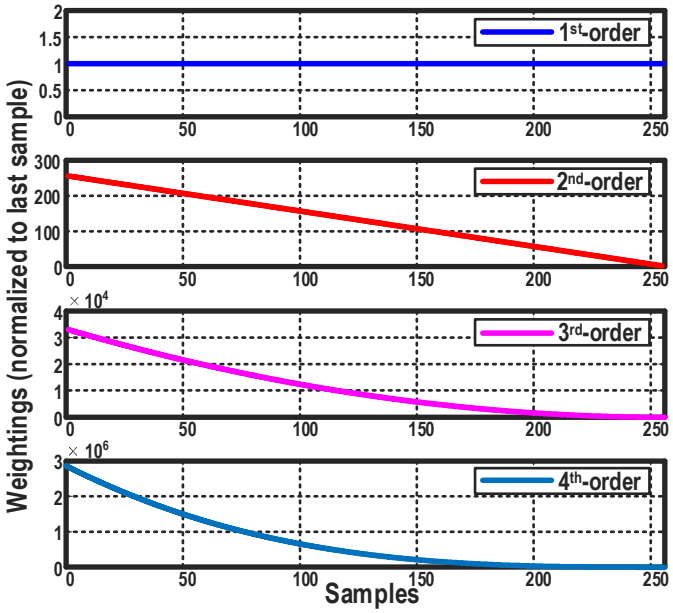

Fig. 5. The weightings of 1[st]- to 4[th]-order IADCs.

where $M=c_1c_2\ldots c_L\cdot N(N+1)(N+2)\ldots(N+L-1)/L!$ is the signal gain of L[th]-order IADC.

The analysis above shows that a high-order architecture can reach high resolution with less conversion cycles [3]. However, the coefficients of the loop filter are restricted to values lower than 1 to guarantee loop stability, which results in the gain attenuation of later conversion cycles.

III. Impacts of Weighting on Performance

a) Impact on Thermal Noise

Thermal noise is a fundamental limiting factor that must be carefully considered in high-resolution ADCs [5]. Different from the quantization noise[1], the thermal noise is random and sample-independent. Compared with the rapid drop of quantization noise during the proceeding of the IADC conversion cycle, the attenuation of thermal noise is relatively slow since it is a kind of "white noise". To suppress the thermal noise to a satisfactory level, a much larger number of conversion cycles is required. As a result, the oversampling technique was often used in signal processing to reduce the thermal noise by the principle of averaging. During the sampling operation, the thermal noise could be regarded as a random signal, which is uncorrelated with the input. Thus, the final SNR would be improved by the oversampling technique, resulting in a 3dB improvement for every doubling of the OSR.

In the first-order IADC, the STF can be written as follow:

$$STF_{1st} = \frac{1}{1-z^{-1}} = 1 + z^{-1} + z^{-2} + z^{-3} + \cdots \quad (7)$$

From Eqs. (7), an important conclusion can be observed: the first-order IADC has uniform weightings, from the first sample to the last one. The input-referred thermal noise can be ideally suppressed by OSR (i.e., the number of conversion cycles N) as:

$$V^2_{n,input_{uniform}} = \frac{2kT}{C_s}\frac{1}{N} \quad (8)$$

Thus, the first-order IADCs will benefit fully from the OSR for the thermal noise without penalty. If multibit DAC is used, then the effectiveness of the DWA can be benefitted fully also from OSR for suppressing DAC nonlinearity in a similar way.

[1]Although quantization "noise" is normally assumed random, indeed it is a result of deterministic action between the input signal and the quantizer's threshold levels. The quantization noise in later samples in IADCs depends on the previous conversion. As a result, the IADC's OSR can suppress the quantization noise in a faster rate (6dB by 2x OSR for first-order IADC). While the thermal noise is truly random and sample-independent, the IADC's OSR suppress the thermal noise in a much slower rate (3dB by 2x OSR).

Table I

Architecture comparison of IADCs

	1st-order	2nd-order	3rd-order	4th-order	Exp (k_e=1/0.5/0.25)	Linear-Exp (k_e=1)
Resolution ($\log_2$)	$\binom{N_1}{1}$	$\binom{N_2}{2}$	$\binom{N_3}{3}$	$\binom{N_4}{4}$	$\sum_{i=1}^{N}(1+k_e)^{N-i}$	$(N_L+1)\cdot 2^{N_E+1}$
N (or OSR) for 20b resolution	N_1=1048576	N_2=1449	N_3=186	N_4=73	N_E=20/32/55	N=256 (246 linear + 10 Exp)
Input referred thermal noise (when N is sufficiently large)	$\frac{1}{N_1}\cdot\frac{2kT}{C_S}$	$\frac{1.3}{N_2}\cdot\frac{2kT}{C_S}$	$\frac{1.8}{N_3}\cdot\frac{2kT}{C_S}$	$\frac{2.3}{N_4}\cdot\frac{2kT}{C_S}$	$\frac{1}{3/5/9}\cdot\frac{2kT}{C_S}$	$\frac{1.03}{N}\cdot\frac{2kT}{C_S}$
Multi-bit DAC+DWA	√	×	××	×××	××××	√

However, high-order IADCs have a thermal noise penalty due to the non-uniform weights in the signal accumulation [3], [30]-[33], and the OSR_{eff} (i.e., the "effective OSR" for thermal noise reduction) will be reduced. The STF of second-order to fourth-order IADCs are calculated in (9) to (11):

$$STF_{2nd} = \left(\frac{1}{1-z^{-1}}\right)^2 = 1 + 2z^{-1} + 3z^{-2} + 4z^{-3} + \cdots \quad (9)$$

$$STF_{3rd} = \left(\frac{1}{1-z^{-1}}\right)^3 = 1 + 3z^{-1} + 6z^{-2} + 10z^{-3} + \cdots \quad (10)$$

$$STF_{4th} = \left(\frac{1}{1-z^{-1}}\right)^4 = 1 + 4z^{-1} + 10z^{-2} + 20z^{-3} + \cdots \quad (11)$$

It is observed in Eqs. (9) to (11) that higher-order IADCs lead to non-uniform weightings. The earlier inputs earn larger weightings, while the weightings of the later inputs are relatively small.

Fig. 5 shows the uniform weighting of the first-order IADC and non-uniform weightings of the second- to fourth-order IADCs vividly. The non-uniform weightings in the higher-order IADCs are due to the cascaded integrator gains within a single conversion cycle, which makes the earlier samples and residues receive a gain larger than 1 when they are circulated in the integrators every clock cycle. Note that when there is attenuation in the integrator path of the loop, the weightings may vary, but the overall trend remains.

The monotonic decreasing weighting in traditional high-order IADCs results in a thermal noise penalty when we try to use the oversampling technique to suppress the thermal noise. The averaging effect is diminishing due to the reduced weight contributions for the later samples. Thus the "effective OSR", OSR_{eff} [37], [38] on the thermal noise reduction will be reduced. The input-referred noise of such a converter could be calculated as:

$$V^2_{n,input_{non_{uniform}}} = \frac{V^2_{n.total}}{M^2} = \frac{2kT}{C_s}\frac{\sum_{i=1}^{N} W(i)^2}{[\sum_{i=1}^{N} W(i)]^2} \quad (12)$$

where $V_{n.total}^2$ is the total output noise and M is the total gain of the input signal accumulation. $W(i)$ is the weight of the i^{th} sampled data.

Higher noise penalty will happen in higher loop order due to the sharply dropped weightings of later samples. The penalty factor [33], [38] can be described as:

$$penalty\ Factor = N\frac{\sum_{i=1}^{N} W(i)^2}{[\sum_{i=1}^{N} W(i)]^2} \quad (13)$$

where the selected weightings in (13) depend on specific implementations.

For second- to fourth-order IADCs, the calculated thermal noise penalty factors are 1.3/1.8/2.3 when N is sufficiently large. Table I compares the thermal noise penalties from the first- to fourth-order IADCs and the required N=OSR needed to resolve 20 bits. The above penalty discussion holds similarly for using the DWA averaging effect on the multibit DAC nonlinearity reduction in IADCs.

The unity-gain bandwidth of an op-amp is usually limited by process, and as a result, the achievable sampling frequency is limited. Implementing a first-order IADC is tough for its long conversion cycles, leading to extremely high OSR. As shown in Table I, to achieve a resolution of 20-b, the OSR should be larger than 1048576 for a first-order structure. This might not be a good solution for audio bandwidth. Still, in DC to low frequency (tens of Hz) application [3], a first-order IADC with a reasonable sampling frequency and zero noise penalty can be obtained due to the uniform weightings.

A high-order structure can significantly reduce the number of conversion cycles. However, it causes non-uniform sample weightings, resulting in a large thermal noise penalty, as shown in Table I. Furthermore, larger sampling capacitors are needed for the same input-referred thermal noise in higher order, causing more power consumption to drive the increased capacitors.

b) Impact on DAC Mismatch Error

Multibit quantizers are beneficial for SQNR boosting [30], [31], as the final residue is bounded by a smaller quantizer's step size. Besides, it can lead to a power-efficient op-amp topology due to the reduced integrator swing. However, the multibit feedback DAC induces nonlinearity issues due to element mismatches. Since such errors add directly to the modulator's input, the linearity of the DAC must satisfy the overall performance of the IADC. Linearization techniques such as dynamic element matching (DEM) can be realized with a small cost in circuit complexity, especially for the DWA technique.

However, the effectiveness of the DWA has degraded in high-order incremental ADCs because of the non-uniform weightings [30], [31]. Take the second-order structure for example, the weights of DAC are time-varying during conversion, which is the same as the input signal weightings. The earlier input signal and DAC receives a larger gain or weighting. Meanwhile, the various DAC capacitors can be described as:

$$C_i = \overline{C_u}(1 + \varepsilon_i) \quad (14)$$

where $\overline{C_u}$ is the average capacitance value and ε_i represents the mismatch error in the i^{th} unit. Considering the linearly-varied weighting in the second-order IADC, the weighting of DAC error caused by the mismatch in the j^{th} cycle is presented as:

$$W_j = N - j \quad (15)$$

Then, at the end of the N^{th} conversion cycle, the total injected mismatch error is:

$$\varepsilon_{tot} = \sum_{j=1}^{N-1} W_j \times \left(\sum_{i=1}^{D[j]} \varepsilon_i\right) \quad (16)$$

where $D[j]$ is the code of the quantizer.

At the beginning of conversion, the signal, as well as the DAC, has the largest weighting, and the impact of injected mismatch error is more significant. Since the mismatch error has a sample-variant weighting function, rotation of the capacitor array is not effective in suppressing the mismatch errors [30], [31], causing a DWA effectiveness penalty factor similar to that for thermal noise.

IV. Algorithms based on Exponential IADC

a) Exponential IADC Fundamentals

For the conventional IADCs, higher-order structures lead to faster accumulation speed. In first-order IADCs, the weighting of each sample is uniform [2], [37], [38], so the accumulation is the slowest. As the order increases, the weightings of the earlier samples are much larger than the later ones, which makes the IADC achieve higher resolution with smaller conversion cycles. Indeed, the exponential IADC can achieve an extremely fast accumulation speed [37], [38] in a first-order-like structure.

The structure of an exponential IADC and its timing diagram is shown in Fig. 6, where k_e is an exponential coefficient. A larger k_e leads to a faster accumulation speed.

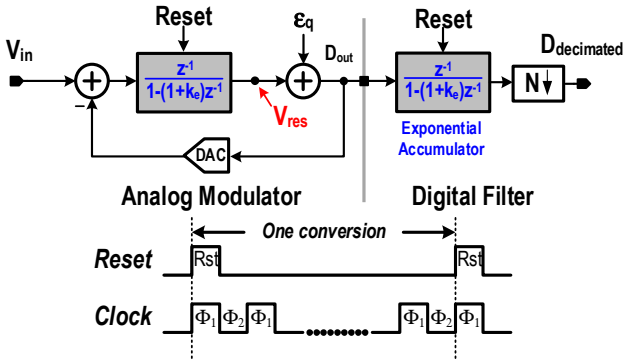

Fig. 6. Diagram of an exponential IADC and its timing [38].

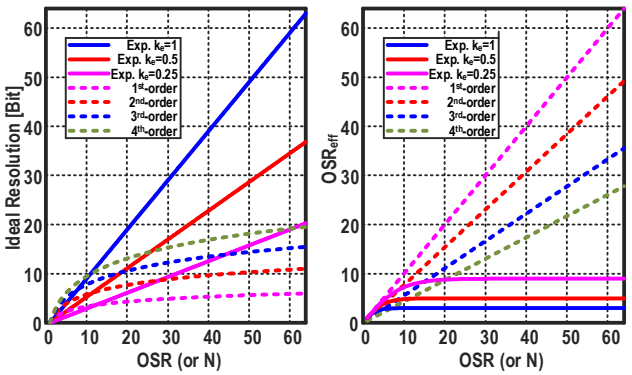

Fig. 7. (a) Theoretical resolution of an exponential IADC and conventional order-based IADCs vs. OSR (or N). (b) Effective OSR of thermal noise reduction of exponential IADC and conventional order-based IADCs vs. OSR (or N) [38].

It is easier to analyze an exponential IADC in the time domain. Once the system is reset, the modulator and digital filter accumulate the difference between the analog input and output of the feedback DAC. It is easy to write the STF in a more obvious way as:

$$STF_{exp} = \frac{1}{1-(1+k_e)z^{-1}}$$
$$= 1 + (1+k_e)z^{-1} + (1+k_e)^2 z^{-2} + (1+k_e)^3 z^{-3} + \cdots \quad (17)$$

It can be seen from (17) that the weighting drops exponentially, in which the larger k_e brings a faster drop. If the weights are normalized to the last sampled signal, the weight of the i^{th} sample is described as:

$$W(i) = (1+k_e)^{N-i} \quad (18)$$

and the total gain of the input signal is as:

$$M = \sum_{i=1}^{N} W(i) = \frac{(1+k_e)^N - 1}{k_e} \approx \frac{(1+k_e)^N}{k_e} \quad (19)$$

Assume that there are L levels in the quantizer and the V_{FS} is the full-scale reference voltage. The height of each step of the quantizer is presented as:

$$V_{refm} = \frac{V_{FS}}{L-1} \quad (20)$$

Then the input voltage can be estimated in (21), in which $V_{res(N)}$ is the residue voltage of the integrator output.

$$\overline{V_{in}} = \frac{\sum_{i=1}^{N} D_{out}[i] V_{refm} W(i)}{M} + \frac{V_{res}(N)}{M} \quad (21)$$

The resolution, in theory, is described as:

$$R = \log_2[M(L-1)] \approx \log_2\left(\frac{(1+k_e)^N}{k_e}\right) + \log_2(L-1) \quad (22)$$

From (22), we can obtain that higher OSR, larger coefficient k_e, and more quantizer levels will bring a higher resolution. Suppose a two-level quantizer is used, Fig. 7 compares the ideal resolution and OSR_{eff} between exponential IADC and conventional order-based ones. The IADCs accumulate signals in a much faster way. To achieve a resolution of 20-b, second- to fourth-order IADCs need 1449/186/73 OSR, respectively, while exponential structures only need 55/32/20 cycles with k_e=0.25/0.5/1 respectively [38].

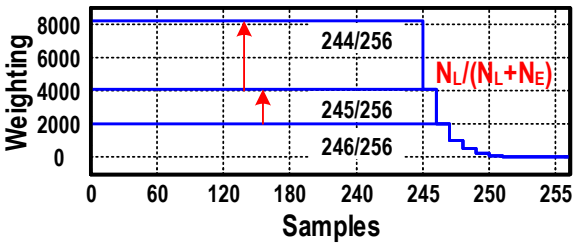

Fig. 8. Weighting function of a linear-exponential IADC with the coefficient k_e of 1 (normalized from the last sample) [38].

Even though the exponential IADC can achieve high resolution via a few conversion cycles, it suffers from the thermal noise penalty because of the non-uniform weightings as high-order IADC does, but in a much more severe way.

After a whole conversion period, the total thermal noise injected by all cycles can be described in (23) and also shown in Table I:

$$V_{n,tot}^2 = \frac{2kT}{C_s}\sum_{i=1}^{N}(1+k_e)^{2N-2i} = \frac{2kT}{C_s}\frac{(1+k_e)^{2N}-1}{k_e(k_e+2)} \quad (23)$$

Then, the input-referred thermal noise can be calculated as:

$$V_{n,in}^2 = \frac{V_{n.tot}^2}{M^2} = \frac{2kT}{C_s}\frac{(1+k_e)^{2N}-1}{k_e(k_e+2)}\frac{{k_e}^2}{[(1+k_e)^N-1]^2} \approx \frac{2kT}{C_s}\frac{1}{1+\frac{2}{k_e}} \quad (24)$$

After a few conversion cycles, the input-referred thermal noise becomes almost unrelated to the increasing number of conversion cycles because of the exponentially decaying weights for later samples. As Fig. 7 (b) presents for exponential IADCs, when OSR increases, the OSR_{eff} remains almost constant in a minimal value, which means that the conversion cycles do not suppress input-referred thermal noise anymore. The situation is even tougher than the high-order conventional IADCs.

The exponential IADCs bring more non-uniform weightings than order-based ones, which get more significant DAC mismatch errors than regular high-order IADCs. With the increase of OSR, the weights drop exponentially, which reduces the effectiveness of DWA as well.

b) Linear-Exponential IADC Algorithm

Based on the linear weightings of first-order IADCs and accelerated accumulation of exponential IADCs, the linear-exponential algorithm was proposed in [34]-[38]. This solution takes advantage of the ideal thermal noise suppression and DWA-friendliness in first-order and fast SQNR boosting in the exponential structure.

The system first works in a linear phase as a first-order IADC to suppress thermal noise as well as to put DWA to work effectively. Although the first-order IADC's uniform weighting brings many advantages to data conversion, its long conversion cycles limit its bandwidth. The origin of such a long conversion is due to the suppression of the large quantization noise. As a result, one can turn the IADC into an exponential phase during the last few conversion cycles in a conversion period to boost SQNR in a short conversion time. With a reasonable distribution of conversion cycles between the first-order and exponential modes, the new algorithm can take advantage of both phases.

The STF of the linear phase is described in (7). In the exponential phase, the STF can be described as (17). Normalize the weights from both linear and exponential phases to the last sample, and the equation in (25) and (26) will be obtained.

$$W(i) = \begin{cases} (1+k_e)^{N_E}, & i \in [1, N_L] \\ (1+k_e)^{N-i}, & i \in [N_L+1, N] \end{cases} \quad (25)$$

$$N_L + N_E = N \quad (26)$$

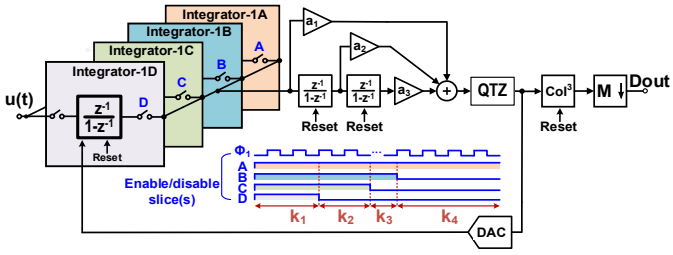

Fig. 9. The 3rd-order IADC with sliced integrator [32], [33].

where N_L and N_E are conversion cycles for linear and exponential phases, respectively. It can be observed in (25) that in the exponential phase, the weights are highly non-uniform and are the same as the situation in exponential IADC. To trade off between high linearity and fast accumulation, there shouldn't be many conversion cycles in the exponential phase.

Suppose k_e=1, the normalized weightings are shown clearly in Fig. 8. Higher weightings will be obtained in the linear phase with more exponential conversion cycles. However, too few cycles in the linear phase will lead to trouble with input-referred thermal noise, so just a few cycles of the exponential phase should be chosen, enough to suppress the quantization noise to a satisfactory level.

To achieve a resolution of 20-b, suppose the total number of conversion cycles is N=256, and the cycle in the linear phase is N_L=246. The thermal noise penalty factor can be calculated based on (13), which is 1.03 [38], almost equal to 1, proving that the linear-exponential algorithm can suppress thermal noise effectively like the first-order IADCs.

In summary, the linear-exponential algorithm takes advantage of the uniform weightings in first-order structure and accelerated accumulation in exponential IADC to get a low thermal noise penalty factor, easy DWA, and fast conversion while avoiding the disadvantages of slow accumulation in the first-order and catastrophic thermal noise/DAC mismatch penalty in exponential IADC.

V. Algorithms based on Exponential IADC

We can see from the above discussion, non-uniform weights in IADCs bring general disadvantages to the high-order and exponential structures. However, with such a unique property, one can take advantage by intentionally utilizing such non-uniform weights in handling the tradeoffs between the quantization noise, thermal noise, DAC mismatches sensitivity, and also power consumption. The following design examples illustrate the concept.

a) IADC with Integrator Slicing

In IADCs, considering the power consumption is dominated by the first integrator because of thermal noise, a reconfigurable slicing-integrator technique was proposed in [32], [33] based on the non-uniform weightings in high-order IADC, which is shown in Fig. 9. This is one of the excellent examples to take advantage of non-uniform weights for power saving in integrators.

The IADC uses a third-order feedforward structure with a two-level quantizer to avoid the DAC mismatch issue, whose OSR is 150 and uses a sampling frequency of 30MHz. The first integrator is divided into four slices, which means each sampling and integration capacitors are divided into four parts with the same size, and the width of MOSFETs in the op-amp is divided by four. Each slice is controlled independently within the cycles from k_1 to k_4 in the timing diagram in Fig. 9, while $k_1/k_2/k_3/k_4$ are 40/30/10/70 respectively.

Contrary to first-order IADC, as the conversion cycle grows, the weightings of third-order IADC drop. Once the resettling signal acts on the system, the early-input samples have large weightings, and four slices of integrator work together in k_1 to take advantage of larger input signal power and lower thermal noise in the integrator. As the conversion continues, the weightings drop, resulting in lower input signal power. Then, the performance requirements of the first integrator become not that high anymore, especially in the aspects

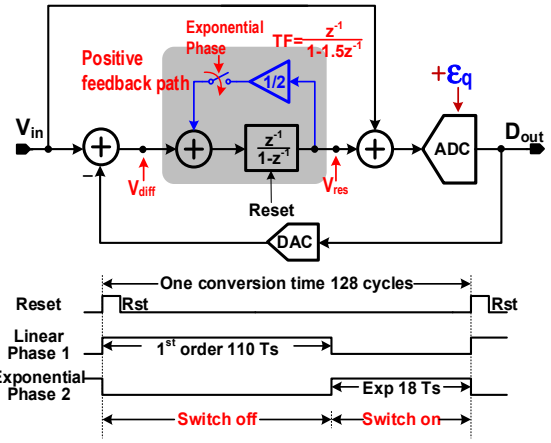

Fig. 10. IADC using conventional integrator with positive feedback and its timing diagram [34].

of thermal noise. Three slices are used in k_2 to guarantee the SQNR while reducing power consumption. Then, it turns into two slices in k_3. Finally, near the end of the conversion period in k_4, the weightings of input samples become relatively small, and large sampling capacitors are not required to suppress thermal noise. Thus, the performance demands of the op-amp become lower. In this situation, only one slice is needed to complete the conversion operation. Such an arrangement is not possible if first-order IADCs are used.

For a third-order IADC, around 80% of power consumption is caused by the first integrator, so reducing the power consumption of the first integrator is the most efficient way to optimize the overall power performance.

From the overall measurement results in [32] and [33], if no integrator-slicing technique is used, the SNR and SNDR are 88.0dB and 87.4dB, respectively, and the power consumption is 1.65mW. After turning on the slicing technique, the SNR and SNDR dropped 0.7 and 0.8dB, respectively, but the power consumption became 33.3% lower. This led to a Schreier figure of merit (FoMS) 0.96dB higher than before.

The thermal noise penalty factor is 1.788 if no slicing technique is used. With the sliced integrators, assume that the sampling capacitance in the k_1 stage is C_s. Then, in $k_1/k_2/k_3/k_4$, the sampling capacitances are $C_s/0.75C_s/0.5C_s/0.25C_s$ respectively, resulting in a thermal noise penalty factor of 2.051. In theory, the SNDR should drop $10\log_{10}(2.051/1.788)$=0.595dB with sliced integrators, which is consistent with the measurement results. The integrator-slicing technique is a good solution that sacrifices little thermal noise penalty to promote much higher power efficiency. There is no DWA effectiveness penalty with the single-bit quantizer.

This work used an integrator-slicing technique based on the non-uniform weightings to achieve an energy-efficient third-order IADC in 180nm CMOS under the supply voltage of 3V. The system achieved an SNDR of 86.6dB and a power consumption of 1.098mW in a bandwidth of 100kHz. The system finally reached an FoMS of 166.2dB [32], [33].

b) IADCs with Positive Feedback

To introduce exponential weightings in IADC, a positive feedback loop is added between the output and input of the integrator in [34]-[36].

As shown in Fig. 10, in [34], the positive feedback path is disabled during the first-order linear phase and activated during the exponential phase. Assume V_{diff} is the difference between the input analog signal and feedback voltage from DAC, and V_{res} is the residue voltage. In the exponential phase, the transfer function can be obtained as:

$$\left[V_{diff}(z) + k_e V_{res}(z)\right]\frac{z^{-1}}{1-z^{-1}} = V_{res}(z) \quad (27)$$

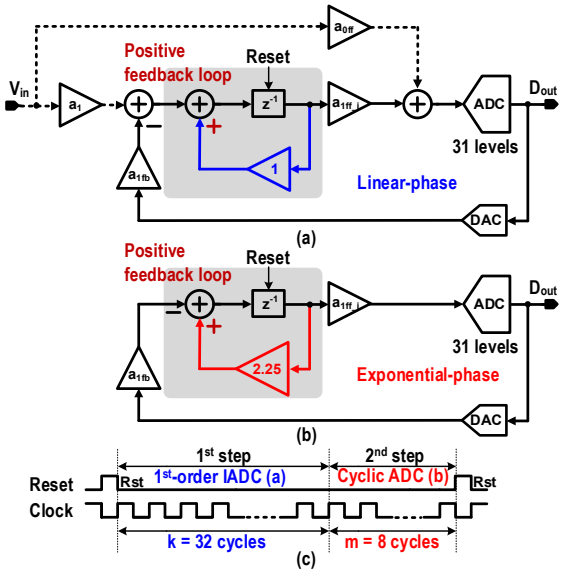

Fig. 11. IADC with positive feedback and cyclic ADC in (a) linear phase and (b) exponential phase and (c) its timing [35], [36].

which can be transformed into:

$$STF_{PF} = \frac{z^{-1}}{1-(1+k_e)z^{-1}} \tag{28}$$

In the work of [34], k_e was selected as 0.5. During 128 conversion cycles with 18 exponential ones, the thermal noise, as well as the DWA penalty factor, is 1.131 according to (13), which is 0.131 larger than the ideal factor of the first-order structure.

The linear-exponential IADC with positive feedback in [34] achieved a peak SNDR of 86.02dB in a 65nm CMOS process under the supply voltage of 1.2V. Working with a sampling frequency of 128MHz, the IADC got a bandwidth of 500kHz, power consumption of 20mW, and an FoMS of 160dB.

Another linear-exponential IADC was proposed in [35], [36] based on a positive feedback loop and cyclic ADC, which is shown in Fig. 11. A high-resolution flash ADC and a multibit DAC are used to reduce the swing of the op-amp and relax the errors in the second stage. In the first step, the IADC works in the first-order mode with uniform and large weightings to suppress input-referred thermal noise and make the DWA effective. Then, it turns into a cyclic ADC with reconfigured positive feedforward loop. The STF during the second step can be calculated as:

$$STF_{cyc} = \frac{1}{1-(1+1.25)z^{-1}} \tag{29}$$

It is apparent from (29) that weightings in the second step are exponential, in which the coefficient k_e is 1.25. Unlike the linear-exponential structure in [34], there is no input analog sampling during the exponential phase in cyclic mode, resulting in no contribution to suppressing thermal noise in the exponential phase. The conversion cycle of the first step is selected as 32 and the second step as 8. Since the input-referred thermal noise is only suppressed in the linear phase, the equivalent penalty factor is observed to be 1.190 for thermal noise and 1.199 for DWA effectiveness.

The IADC based on cyclic ADC and positive feedback in [35] and [36] was designed in a 180nm process under a supply voltage of 3V. The power consumption was 27.7mW. With a bandwidth of 625kHz and SNDR of 96.6dB, the IADC reached an FoMS of 170.1dB.

c) Linear-Exponential IADC with Noise Coupling

The implementation of exponential integration in [34]-[36] relies on positive feedback, which degrades the integrator feedback factor. To solve this problem, the noise-coupled structure was proposed in [37] and [38] to implement linear-exponential IADC.

It can be observed in Fig. 12 that noise coupling can be implemented via an improved error feedback circuit. The quantization noise ε_q can be obtained in the analog domain by

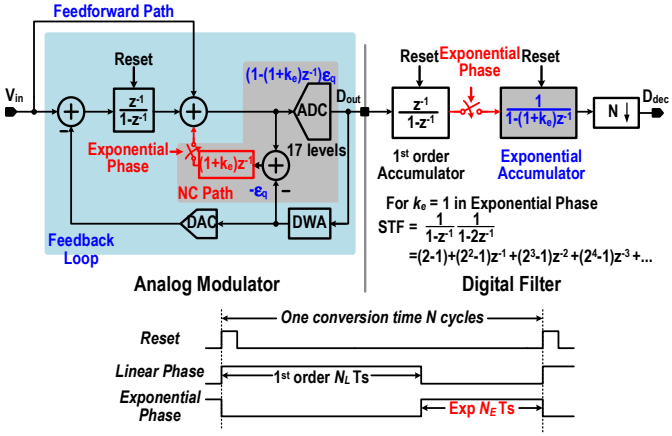

Fig. 12. IADC using noise-coupling technique [37], [38].

subtracting the internal quantizer input from the output digital signal. The quantization noise is then transported to the input of the quantizer with a delay of 1 clock cycle. Notice that the quantization noise is scaled by $(1+k_e)$, resulting in an equivalent quantization noise of $[1-(1+k_e)z^{-1}]\varepsilon_q$, and the analog exponential integrator with noise-coupling is mapped in the digital domain in the form of a decimation filter. Compared with linear-exponential IADCs with positive feedback, this structure has less power penalty since the extra noise-coupling capacitors and adders are added in the backend and consume less power and area.

The STF in the exponential phase in the noise-coupling structure differs from what it was in the positive feedback structure since the loop filters are equivalent to being cascaded with a conventional integrator and an exponential one. The STF is shown as:

$$STF_{NC} = \frac{1}{1-z^{-1}}\frac{1}{1-2z^{-1}}$$
$$= (2-1)+(2^2-1)z^{-1}+(2^3-1)z^{-2}+(2^4-1)z^{-3}+\cdots \tag{30}$$

which can be regarded as exponential weightings approximately. The penalty factors of thermal noise and DWA effectiveness in are both 1.034.

The use of noise-coupling in IADCs also has additional benefits in the multibit DAC nonlinearity, as the noise-coupling equivalently acts as a dither for the quantizer, which is also demonstrated in [40] and [40].

The noise-coupled linear-exponential IADC in [37] and [38] was designed in a 65nm process under the supply voltage of 1.2V. With a sampling frequency of 10.24MHz and a bandwidth of 20kHz, the IADC achieved a peak SNDR of 100.8dB with a power consumption of 550μW. An FoMS of 176.4dB is finally obtained.

d) 3rd-order IADC with Reconfigurable Quantizer

Multibit oversampling converters are well-known for their problems in multibit DAC nonlinearity. Traditionally, techniques like the DWA [29] or DAC calibration [42] are utilized to mitigate such issues. Also, [43] demonstrated an example of using tailor-made architectural innovations to suppress the DAC mismatches, making the multibit oversampling converter free from DWA/DAC calibration. In the example below, we can see that DWA/DAC calibration-free implementation is also possible through architectural advances with non-uniform weightings in high-order IADCs.

A 3-0 sturdy-multi-stage noise-shaping (SMASH) continuous-time (CT) IADC with reconfigurable quantizers was proposed in [30] and [31], which is shown in Fig. 13. The quantizers are implemented by a reconfigurable multibit asynchronous (A) SAR ADC, which can be switched between 2-b and 5-b modes to suppress the nonlinearity of DAC mismatches according to the non-uniform weightings of third-order IADC and bring high linearity to the system. The DAC is utilized with 1.5b- to 4b tri-level output switching.

After the reset signal is applied to the system, the incremental SMASH ADC works in a high linearity 1b-1b mode for 40 cycles (3-0 SMASH, with 1b in the first stage of third-order and 1b in the second

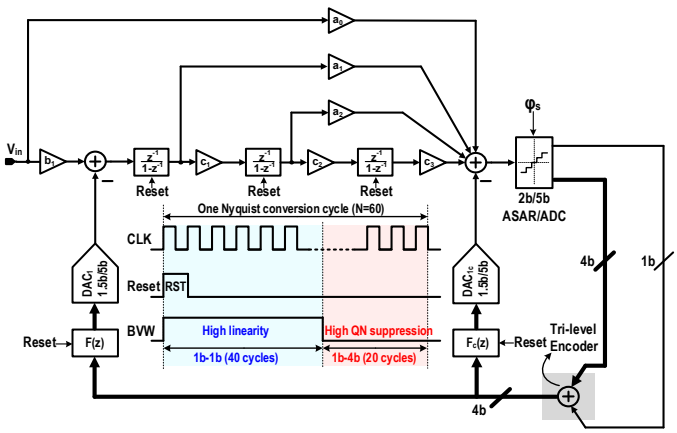

Fig. 13. Diagram and timing of the 3-0 SMASH IADC [30], [31].

Table II

Comparison of Discussed IADCs

Reference	P. Vogelmann ISSCC-18 [32] JSSC-19 [33]	B. Wang ASSCC-19 [34]	T. Katayama VLSI-18 [35] SSCL-18 [36]	B. Wang VLSI-18 [37] JSSC-19 [38]	M. A. Mokhtar CICC-21 [30] JSSC-22 [31]
Architecture	DT-IADC Slicing Integrator	DT-IADC Linear-Exp Positive FB	DT-IADC Linear-Exp Positive FB	DT-IADC Linear-Exp Noise- Couple	CT-IADC 3-0-SMASH ASAR-VBW
Process (nm)	180	65	180	65	28
Supply (V)	3	1.2	3	1.2	0.9
Frequency (MHz)	30	128	55	10.24	120
Bandwidth (kHz)	100	500	625	20	1000
Power (mW)	1.098	20	27.7	0.55	3.6
Peak SNDR (dB)	86.6	86.02	96.6	100.8	81.2
DR (dB)	91.5	94.6	100.1	101.8	89
Thermal noise penalty factor	1.788* /2.051**	1.131	1.190	1.034	1.771
DWA effectiveness penalty factor	N/A+	1.131	1.199	1.034	N/A++
$FoM_{s,SNDR}$(dB)#	166.2	160.0	170.1	176.4	165.6
$FoM_{s,DR}$(dB)##	171.1	168.6	173.6	177.4	173.4
Area (mm^2)	0.363	0.26	0.72	0.13	0.125

* Thermal noise penalty factor without slicing technique;

** Thermal noise penalty factor with sliced integrators while $k_1:k_2:k_3:k_4$=40:30:10:70;

+ A single-bit quantizer is used in this work, so there is no DAC mismatch;

++ SMASH structure and tri-level encoding make it incomparable with single-loop IADCs;

$FoM_{s,SNDR}$=SNDR+10log$_{10}$(BW/Power); ## $FoM_{s,DR}$=DR+10log$_{10}$(BW/Power).

stage of zeroth-order). The previous analysis of high-order IADC is also suitable for incremental SMASH ADC. In a third-order structure, the non-uniform weightings for early-sampled data are relatively high. As a result, 1b DAC is utilized in this high-linearity phase, resulting in no DAC mismatch contribution in the early samples with higher weights. As conversion enters the high quantization noise suppression phase of 20 cycles, the DAC is reconfigured to 4b mode. The weightings under this mode drop sharply, and the mismatches in 4-bit DAC's impact on the system reduce. With the sharply reduced weightings, the nonlinearity of multibit DAC caused by mismatches is suppressed. The least significant bit (LSB) of 4b operation can lead to small residue quantization noise. Thus, this IADC achieved a DWA/calibration-free multibit DAC implementation from the architecture level. The thermal noise penalty factor is 1.771 for a third-order structure.

Notice that the SMASH structure in [30] and [31] utilized a tri-level encoder, which implies a different consideration in DAC sensitivity. Thus the DWA penalty factor is not calculated in Table II.

It is worth noting that since the weightings drop more sharply in higher conversion cycles, the technique of reconfigurable quantizer and DAC is more effective with larger OSR. Furthermore, this technique is effective with non-uniform weightings, which is not helpful for first-order structure, similar to the IADC with the sliced integrator.

The 3-0 incremental SMASH ADC in [30] and [31] was implemented in a 28nm process. The power consumption of the total system is 3.6mW under a 0.9V supply voltage. The system achieved a peak SNDR of 81.2dB with a sampling frequency of 120MHz and OSR of 60, showing the insensitivity of the DAC mismatches without any DAC linearization techniques (DWA/calibrations). The achieved FoMs was 165.6dB.

VI. Conclusions

The IADC architectures are getting more attention nowadays for their outstanding performance in weak-signal detection, multi-channel multiplexing capability and other high-resolution application scenarios. This review paper described the basic order-based IADC structures. Then the concept of weightings was introduced to explain its influence on thermal noise and DAC mismatches, which are the two major problems that limit the performance of IADCs, and then led to the concept of penalty factor. The algorithm of exponential IADC was explained to obtain accelerated accumulation contrary to long conversion cycles in order-based IADCs. To improve the catastrophically degraded thermal noise penalty factor in exponential IADC, the linear-exponential algorithm was presented. The algorithm takes advantage of linear weightings in the first-order phase to reduce slowly decreased thermal noise to a satisfying degree and accelerated accumulation in the exponential phase to suppress the quantization noise in a few conversion cycles quickly. Then we discussed several design examples taking advantage of weighting to reduce power consumption, and improve the performance over thermal noise and DAC mismatches. The performances of discussed works are summarized and compared in Table II. These examples clearly show that the non-uniform weighting function in IADCs can be a good tool for optimizing the performance of IADCs.

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