A 266-μW Bluetooth Low-Energy (BLE) Receiver Featuring an N-Path Passive Balun-LNA and a Pipeline Down-Mixing BB-Extraction Scheme Achieving 77-dB SFDR and -3-dBm OOB-B$_{-1\,\mathrm{dB}}$

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***Abstract*— This article reports an ultra-low-power (ULP) Bluetooth low-energy (BLE) receiver with an improved spurious-free dynamic range (SFDR). It features two passive-intensive RF techniques: an N-path passive balun-LNA and a pipeline down-mixing baseband (BB)-extraction scheme. They together offer a high-Q bandpass response at RF, and a high passive gain to suppress the noise of the BB hybrid complex filter. Specifically, the balun-LNA is a step-up triple-coil transformer aided by an N-path switched-capacitor (SC) network to perform in-band voltage amplification, high-Q bandpass filtering, I/Q down-mixing, and input-impedance matching. Instead of using active amplifiers as the first-BB gain stage, we passively extract the four-phase (I/Q and differential) BB signals using a pipeline of passive-SC networks that can stack up the voltage gain. Prototyped in TSMC 28-nm CMOS, the BLE receiver consumes only 266 μW, of which 75 μW in the BB hybrid filter at 1 V, and 191 μW in the LO divider + buffer at 0.6 V. Measured at the maximum RF-to-BB gain of 61 dB, the receiver exhibits a noise figure (NF) of 6.1 dB and an out-of-band (OOB)-IIP$_3$ of 22.5 dBm. The corresponding SFDR is 77 dB for a 1-MHz BLE channel and a 10-dB minimum signal-to-noise ratio (SNR$_{\mathrm{min}}$). The OOB-B$_{-1\,\mathrm{dB}}$ is -3 dBm.**

***Index Terms*— Balun-low-noise amplifier (balun-LNA), bandpass filtering, baseband (BB), Bluetooth low-energy (BLE), CMOS, hybrid filter, noise figure (NF), nonlinearity, N-path, out-of-band (OOB), passive gain, pipeline, spurious-free dynamic range (SFDR), ultra-low-power (ULP).**

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I. Introduction

ULTRA-LOW-POWER (ULP) short-range radios are the cornerstone of building a world with Internet-of-Everything connectivity. Electronic gadgets, such as wireless earbuds, can enjoy an extended battery life by minimizing the radio power consumption. Practically, the coexistence of multiple wireless standards (e.g., Wi-Fi, ZigBee, and Bluetooth) in the 2.4-GHz industrial scientific medical (ISM) band challenges the sub-mW radio design that has to possess both high sensitivity and high blocker resilience. They, translated into the circuit level, require a parallel improvement of the noise figure (NF) and out-of-band (OOB) IIP$_3$ that together govern the spurious-free dynamic range (SFDR) of a receiver. A high SFDR implies a higher capability to uphold a minimum signal-to-noise ratio (SNR$_{\mathrm{min}}$) for the back-end demodulator in the presence of blockers.

To secure a high sensitivity at a sub-mW power budget, the state-of-the-art Bluetooth low-energy (BLE) receivers [1], [2], [3], [4], [5], [6] commonly employ an active RF front-end involving at least one gain stage (transconductance g_{m}). For example, ultra-low-voltage (ULV) LNAs in [1] and [2] succeed in power savings, but the squeezed voltage headroom tightens the tradeoff between the NF, linearity, and gain-compression point. The LNA in [1] only achieves a -3.5 dBm OOB-IIP$_3$ at a 240-μW power budget and a 28.9-dB gain. The current-reuse LNA-mixer-VCO (LMV) cell [3] reduces the power budget by sharing one bias current between more functions. Yet, it suffers from similar issues as in [2], and is prone to block-to-block crosstalk. The mixed-voltage design [4], [5] is an alternative to tailor the supply voltages for the RF and baseband (BB) circuits, but it demands extra efforts from the power-management circuits. In [6], recycling one block for multiple functions can reduce the numbers of bias currents without losing the voltage headroom. Yet, the noise and nonlinearity penalties of the g_{m} remain unsolved. Obviously, the g_{m} can significantly limit the SFDR of an active RF front-end at low power, e.g., <51 dB in [2] and [3] under a sub-0.5-mW power budget. Although the mixed-voltage design in [5] shows a higher SFDR of 59.4 dB, it consumes a larger power (0.58 mW), and requires a dedicated bondwire length at the RF input for the passive pre-gain.

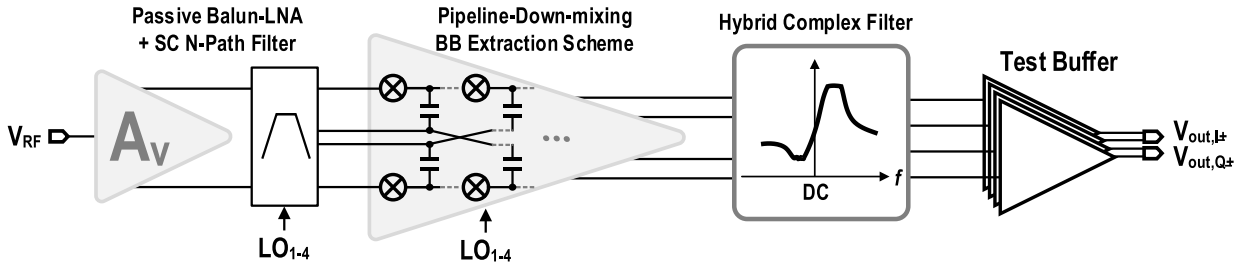

Fig. 1. Proposed ULP BLE receiver using a passive RF front-end to improve the SFDR.

This article details the ULP BLE receiver briefed in [7]. We introduce a passive RF front-end with two key elements: an N-path passive balun-LNA and a pipeline down-mixing BB-extraction scheme. Together they raise the SFDR of the receiver without burdening the power budget. Their key properties are: 1) no g_m nonlinearity; 2) generation of a large voltage gain to suppress the noise of the BB circuitry; and 3) offer a high-Q bandpass characteristic to suppress the OOB blockers.

Fig. 1 overviews the key features of our passive-intensive BLE receiver. It innovates a passive balun-LNA (i.e., a step-up triple-coil transformer) and an N-path switched-capacitor (SC) filter to jointly realize the RF and the first-BB passive gains, without involving any g_m. Sharing the same set of four-phase 25%-duty-cycle LO (LO_{1-4}), the N-path passive balun-LNA and the pipeline down-mixing BB-extraction scheme implement together a high-Q bandpass response at RF with input-impedance matching and a high-voltage gain, thus reducing the power budget and noise contribution of the subsequent hybrid complex filter. The SC N-path filter with $N = 4$ naturally provides the desired four-phase (I/Q and differential) BB signals. To raise the voltage gain, we introduce a pipeline of passive-SC networks that can stack up the voltage gain during the BB extraction. The hybrid complex filter performs image rejection and further signal amplification. It has a complex-pole input impedance enhancing the image-rejection ratio (IRR). The test buffers are the typical source follower for measurement purposes.

Prototyped in TSMC 28-nm CMOS, the BLE receiver scores a 6.1-dB NF and a 22.5-dBm OOB-IIP_3 at a maximum gain of 61 dB. The SFDR is 77 dB for a 1-MHz BLE channel and a 10-dB SNR_{min}. The SFDR and -3-dBm OOB -1-dB gain-compression point (OOB-$B_{-1\,dB}$) are at least 19 dB better than a recent work [8], while consuming 28% less power. The active area is 0.5 mm^2.

After the Introduction, Sections II and III present the details of the two key RF techniques. Sections IV and V describe the hybrid filter and the LO generator, respectively. Section VI summarizes the measurement results, and Section VII draws the conclusions.

II. N-Path Passive Balun-LNA

A. Principle of the N-Path Passive Balun-LNA

Fig. 2 sketches the proposed balun-LNA passively built by a step-up triple-coil transformer rounded by two (differentially)

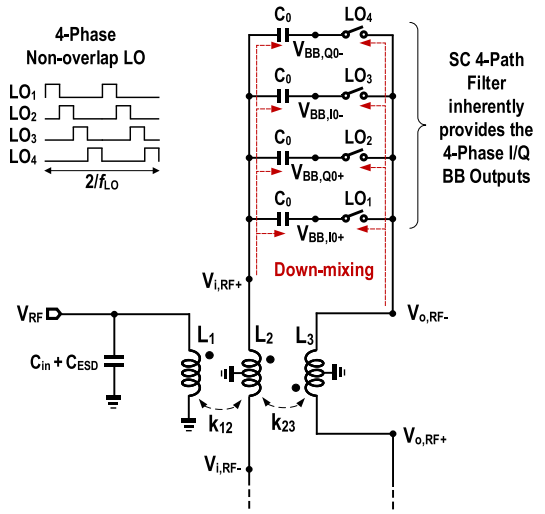

Fig. 2. Proposed N-path passive balun-LNA (simplified). It features a step-up triple-coil transformer to realize the single-ended-to-differential conversion (L_1 to L_2) and passive gain (L_2 to L_3). The SC N-path filter driven by a four-phase non-overlap LO (LO_{1-4}) offers high-Q bandpass filtering and input-impedance matching.

N-path SC networks. The transformer performs single-ended-to-differential conversion (L_1 to L_2) and voltage amplification (L_2 to L_3) in a combined footprint by vertically stacking three spiral coils with various metallization. Parallelizing it with two (differentially) SC N-path filters driven by a set of four-phase non-overlap LO (LO_{1-4}), the transformer will feature a high-Q bandpass response with its center frequency defined by the LO. Without any g_m nonlinearity, the proposed balun-LNA has a primary linearity limit set by the MOS switches, much more linear than the g_m.

By arranging L_2 to L_3 in reverse-coupling, the OOB blockers undergo partial cancellation. The N-path SC network shows a high impedance only at the vicinity of the LO frequency (f_{LO}), while behaves with low impedance at other frequencies. Therefore, we can couple and amplify the IB signal to $V_{o,RF\pm}$ via the transformer, while the OOB blockers pass through both the transformer and the N-path SC network. At $V_{o,RF\pm}$, the circuit will obtain a partial cancellation of the blockers.

Similar to [9], [10], and [11], the passive voltage gain (A_V) provided by the transformer can create a passive Miller effect over the SC N-path filter. This allows the use of smaller switches and capacitors, leading to a small parasitic effect and LO power budget. With $N = 4$ and a four-phase non-overlap LO, the down-mixing exists in the SC N-path filter,

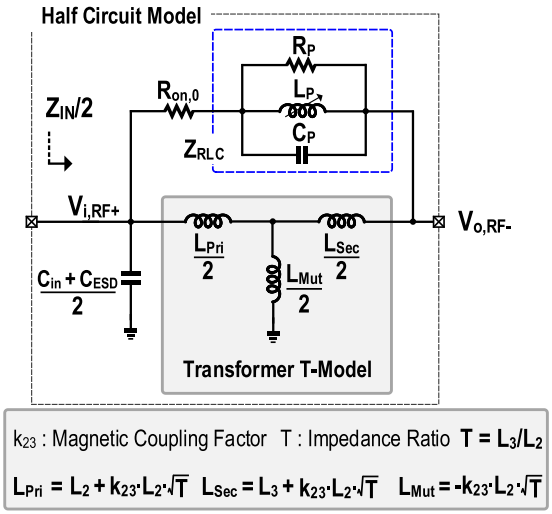

Fig. 3. Half-circuit LTI analytical model of the N-path passive balun-LNA. Transformer replaced by its T model and the SC N-path network replaced by a paralleled RLC network [12].

intrinsically. Then, we can extract the four-phase I/Q BB outputs without extra mixers. Here, the SC N-path filter can down-mix the RF signals at $V_{\mathrm{i,RF}\pm}$ and $V_{\mathrm{o,RF}\pm}$ to the BB plate of C_0 with the same polarity, performing a boosted amplification of $2(1+A_{\mathrm{V}})$. The factor 2 derives directly from the differential outputs.

B. Linear Time-Invariant (LTI)-Based Analytical Model

Fig. 3 presents the LTI-based analytical model of the N-path passive balun-LNA, with the N-path SC network modeled as an equivalent paralleled RLC network (Z_{RLC}) [12]. The transformer, simplified with its T-section model [13], mainly analyzes the voltage amplification function of the secondary (L_2) to the tertiary (L_3) coil, with the primary (L_1) to secondary coil designed for single-ended-to-differential conversion. In the T-section model, composed by L_{Pri}, L_{Sec} and L_{Mut}, L_{Mut} represents the L_2–L_3 mutual coupling. T is the impedance ratio, which is equal to $(L_3/L_2)^2$. Z_{RLC} resonates at f_{LO}, with $R_{\mathrm{P}} = N^2\sin^2(\pi/4)/[\pi^2 - N^2\sin^2(\pi/4)]\cdot(R_{\mathrm{S}} + R_{\mathrm{on,0}})$, $C_{\mathrm{P}} = \pi^2/[\sin^2(\pi/4)]\cdot C_0$ and $L_{\mathrm{P}} = 1/[(2\pi f_{\mathrm{LO}})^2\cdot C_{\mathrm{P}}]$, respectively, [12]. R_{S} is the antenna impedance.

1) Input-Impedance Analysis:: According to the LTI analytical model in Fig. 3, we derive the input impedance as

$$Z_{\mathrm{IN}}(\mathrm{j}\omega_{\mathrm{in}}) = \frac{1}{\mathrm{j}\omega_{\mathrm{in}}\cdot(C_{\mathrm{in}}+C_{\mathrm{ESD}})} \Big\| \frac{(\mathrm{j}\omega_{\mathrm{in}})^2\cdot(1-k_{23}{}^2)TL_2^2 + \mathrm{j}\omega_{\mathrm{in}}\cdot 2L_2Z_{\mathrm{NP}}}{\mathrm{j}\omega_{\mathrm{in}}\cdot(1+T+2k_{23}\sqrt{T})L_2 + 2Z_{\mathrm{NP}}} \tag{1}$$

where $Z_{\mathrm{NP}} = R_{\mathrm{on,0}} + Z_{\mathrm{RLC}}$ represents the effective impedance of the N-path SC network. $R_{\mathrm{on,0}}$ is the ON-resistance of the N-path switch, which dominates the OB impedance. $C_{\mathrm{in}} + C_{\mathrm{ESD}}$ is responsible for the passband centering (detailed later), with C_{ESD} associated with the electrostatic discharge (ESD) protection diodes. After neglecting insignificant terms [i.e., $(\mathrm{j}\omega_{\mathrm{in}})^2\cdot(1-k_{23}^2)TL_2^2$], we can simplify the input impedance as

$$Z_{\mathrm{IN}}(\mathrm{j}\omega_{\mathrm{in}}) \approx \frac{2Z_{\mathrm{NP}}}{(1+T+2k_{23}\sqrt{T})} \approx \frac{2Z_{\mathrm{NP}}}{(1+A_{\mathrm{V}})^2}. \tag{2}$$

$Z_{\mathrm{IN}}(\mathrm{j}\omega_{\mathrm{in}})$, roughly defined by $2Z_{\mathrm{NP}}$ with a scaling factor of $1/(1+T+2k_{23}\sqrt{T})$, is equivalent in a similar way to the Miller effect. Contrasting with the Miller effect obtained with an active amplifier offering the effective impedance with a scaling factor of $1/(1+A_{\mathrm{V}})$ at the input, here, the scaling factor provided by the step-up transformer is $1/(1+A_{\mathrm{V}})^2$ for a perfect coupling factor (i.e., $k_{23} = 0.89$). The effective capacitance at the input node $V_{\mathrm{i,RF}\pm}$ is the physical capacitance of the SC N-path filter multiplied by the loop gain created by step-up transformer, consequently, effectively reducing the capacitor size and the dynamic power.

2) Transfer Function Analysis:: Based on the LTI analytical model, the voltage gain at $V_{\mathrm{o,RF}\pm}$ is

$$\begin{aligned} H_{\mathrm{RF}}(\mathrm{j}\omega_{\mathrm{in}}) &= \frac{V_{\mathrm{o,RF}-} - V_{\mathrm{o,RF}+}}{V_{\mathrm{RF}}} \\ &= \frac{2Z_{\mathrm{IN}}(\mathrm{j}\omega_{\mathrm{in}})}{R_{\mathrm{S}} + 2Z_{\mathrm{IN}}(\mathrm{j}\omega_{\mathrm{in}})} \\ &\quad\cdot \frac{\mathrm{j}\omega_{\mathrm{in}}\cdot(k_{23}^2-1)L_2 + 2k_{23}/\sqrt{T}Z_{\mathrm{NP}}}{\mathrm{j}\omega_{\mathrm{in}}\cdot(k_{23}^2-1)L_2 - 2Z_{\mathrm{NP}}/T}. \end{aligned} \tag{3}$$

In (3), the first part $2Z_{\mathrm{IN}}(\mathrm{j}\omega_{\mathrm{in}})/[R_{\mathrm{S}} + 2Z_{\mathrm{IN}}(\mathrm{j}\omega_{\mathrm{in}})]$ provides the RF bandpass filtering response, whereas the other part provides the passive voltage gain. When neglecting the term $\mathrm{j}\omega_{\mathrm{in}}\cdot(k_{23}^2-1)L_2$ (i.e., $-\mathrm{j}2.69\ \Omega$), we can simplify (3) into (4) with $k_{23} = 0.89$ and $L_2 = 0.86$ nH at 2.4 GHz, namely

$$H_{\mathrm{RF}}(\mathrm{j}\omega_{\mathrm{in}}) = \frac{\frac{G}{Q}\omega_0\cdot\mathrm{j}\omega_{\mathrm{in}}}{(\mathrm{j}\omega_{\mathrm{in}})^2 + \frac{\omega_0}{Q}\cdot\mathrm{j}\omega_{\mathrm{in}} + \omega_0^2} \tag{4}$$

in which, G is the passive voltage gain, ω_0 and Q are the natural frequency and quality factor, defined in (5), (6), and (7), as shown at the bottom of the next page, respectively. For input-impedance matching, R_{S} will be $2R_{\mathrm{P}}/(1+T+2k_{23}\sqrt{T})$ and G becomes $-k_{23}\sqrt{T}$. Besides, ω_0 is consistent with the result in the input-impedance analysis. As expected, (4) inherits the bandpass filtering characteristic of Z_{RLC}. Finally, we arrive to a second-order RF bandpass filtering response at $V_{\mathrm{o,RF}\pm}$ with a voltage gain of $-k_{23}\sqrt{T}$, which fits well with the simulation results shown in Fig. 4

$$G = \frac{-4k_{23}\sqrt{T}R_{\mathrm{P}}}{R_{\mathrm{S}}(1+T+2k_{23}\sqrt{T}) + 2R_{\mathrm{P}}} \tag{5}$$

$$\omega_0 = \sqrt{\frac{(1+T+2k_{23}\sqrt{T})L_2 + 2L_{\mathrm{P}}}{(1+T+2k_{23}\sqrt{T})L_2L_{\mathrm{P}}\left[C_{\mathrm{P}} + \frac{2(C_{\mathrm{in}}+C_{\mathrm{ESD}})}{1+T+2k_{23}\sqrt{T}}\right]}}. \tag{6}$$

For a typical SC N-path filter, the input parasitic capacitance always incurs in a left-shifting of the passband center frequency [12] and [14]. Differently here, our balun-LNA generates a right-side shifting due to the inductive effect (i.e., L_2 and L_3). By organizing (6), the center frequency ω_0 becomes

$$\omega_0 = \sqrt{(\omega_{\mathrm{LO}})^2 + \frac{(\Delta\omega)^2 - (\alpha\omega_{\mathrm{LO}})^2}{1+\alpha^2}} \tag{8}$$

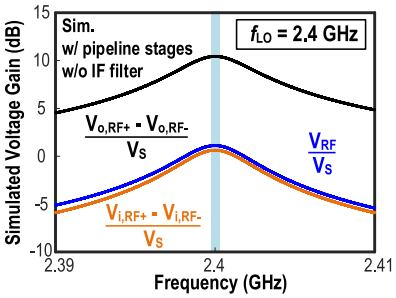

Fig. 4. Simulated high-Q filtering at both input and output of the N-path passive-balun LNA. V_S is the source voltage from the antenna, which is not shown in Fig. 2.

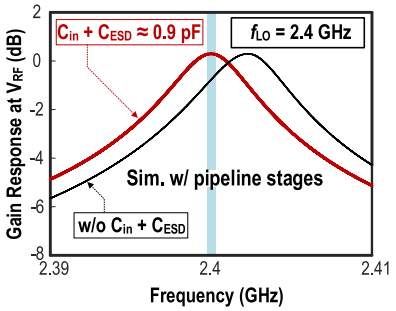

Fig. 5. $C_{in} + C_{ESD}$ compensates the right offset of the passband center frequency. The passband center aligns with the LO frequency.

where $\omega_{LO} = 1/(L_P C_P)^{1/2}$ is the resonant frequency of the RLC network, $\Delta\omega = \{2/[L_2(1 + T + 2k_{23}\sqrt{T})C_P]\}^{1/2}$ represents the right-shifting term and $\alpha = \{2(C_{in}+C_{ESD})/[(1+T + 2k_{23}\sqrt{T})C_P]\}^{1/2}$ is the frequency compensation term. To re-center the passband frequency, we apply a capacitor C_{in} at $V_{i,RF}$, and we also consider C_{ESD}. C_{in} and C_{ESD} create a left-shifting term with an equivalent capacitance of $2(C_{in} + C_{ESD})/(1 + T + 2k_{23}\sqrt{T}) + C_P$ in the RLC network, and with ω_0 finally aligned with ω_{LO}. In the current design, we choose $C_{in} + C_{ESD} \approx 0.9$ pF, which contributes to the alignment of the passband center frequency with f_{LO}, presented also in Fig. 5. C_{ESD} is ~50 fF, which contributes a negligible impact on the input capacitance.

Indeed the down-mixing exists intrinsically in the balun-LNA and we can extract the four-phase I/Q BB signals at $V_{BB,I0\pm}$ and $V_{BB,Q0\pm}$. Two down-mixing paths contribute to the BB outputs (see Fig. 2), with $V_{i,RF+}$(via C_0) and $V_{o,RF}$ (via the N-path switch driven by LO_1) generating the BB signal at $V_{BB,I0+-}$. For a typical N-path SC network, Iizuka and Abidi [15] and [16] detail its RF-to-BB voltage gain response. Similarly, the RF-to-BB voltage gain response is

$$H_{\text{RF-to-BB}}(j\omega_{in}, j\omega_{out}) = [1 - H_{RF}(j\omega_{in})] \cdot \frac{\text{sinc}(\pi/N \cdot \omega_{in}/\omega_{LO})}{1+j\omega_{out}2[R_S+R_{on,0}/(1+T+2k_{23}\sqrt{T})](1+T+2k_{23}\sqrt{T})C_0} \quad (9)$$

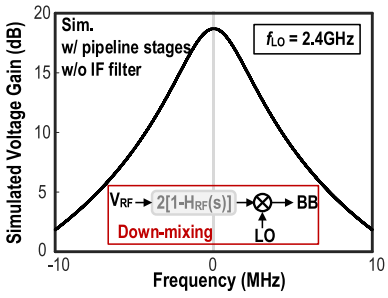

Fig. 6. Simulated RF-to-BB gain response extracted from the N-path passive balun-LNA. Components' parameters: $L_1 = L_2 = 0.86$ nH, $L_3 = 6.02$ nH, $k_{12} = 0.86$, $k_{13} = 0.89$, $C_0 = 2$ pF and switch of 1.2 μm/30 nm.

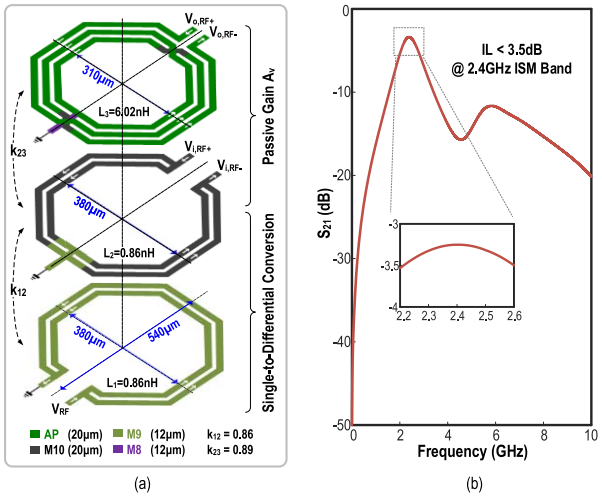

Fig. 7. Proposed (a) vertically stacked step-up triple-coil transformer with different metallization and (b) its EM-simulated S_{21}.

which is the gain response for a single path. In (9), the term $1 - H_{RF}(j\omega_{in})$ reflects the down-mixing behavior from both $V_{i,RF\pm}$ and $V_{o,RF\pm}$ to $V_{BB,I0+}$, and the factor of $1+T+2k_{23}\sqrt{T}$ derives from the passive Miller effect. When considering the kth ($k = 0, 1, \ldots, N-1$) path, we should include the factor $e^{j2\pi k/N}$. With $N = 4$, the differential passband voltage gain at dc frequency is $2\text{sinc}(\pi/4)(1 + k_{23}\sqrt{T})$. We simulate the RF-to-BB gain response from the N-path passive balun-LNA under the conditions with the step-up triple-coil transformer and pipeline stages. Fig. 6 presents the simulation of the differential passband voltage gain exhibiting a center value of 17 dB, with 5.1 dB due to the RF down-mixing.

C. Step-Up Triple-Coil Transformer

Inspired by Shao *et al.* [17] that employs a transformer as a passive-LNA, here we design a step-up triple-coil transformer to provide the essential functions of a balun-LNA. Fig. 7(a) exhibits such transformer. The single-ended-to-differential conversion obtained by the primary (Metal 9,

$$Q = \sqrt{(1 + T + 2k_{23}\sqrt{T})\left[C_P + \frac{2(C_{in} + C_{ESD})}{1 + T + 2k_{23}\sqrt{T}}\right]\left[\frac{1 + T + 2k_{23}\sqrt{T}}{L_P} + \frac{2}{L_2}\right]} \cdot \frac{R_S R_P}{(1 + T + 2k_{23}\sqrt{T})R_S + 2R_P} \quad (7)$$

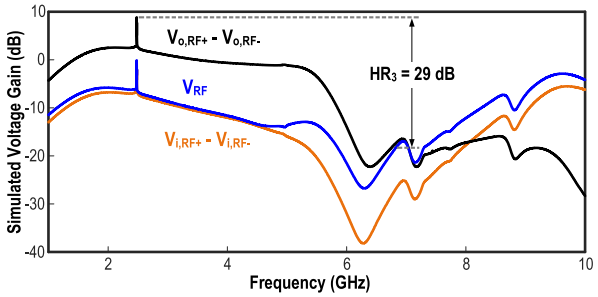

Fig. 8. Simulated wide-view gain response of the N-path passive balun-LNA. The bandpass characteristic of the transformer suppresses the gain at the third RF harmonic (7.2 GHz).

12-μm width) and the secondary (Metal 10, 20-μm width) coils corresponds to the inductance $L_1 = L_2 = 0.86$ nH. The secondary and tertiary (AP, 20-μm width) coils, in which the inductance $L_3 = 6.02$ nH, provide the voltage amplification with an impedance ratio between L_2 and L_3 of 7. By vertically stacking the three spiral coils, the transformer exhibits a high magnetic coupling factor for L_1 and L_2 ($k_{12} = 0.86$), and L_2 and L_3 ($k_{23} = 0.89$). The trace space is 15 μm. From simulation in Fig. 7(b), the insertion loss of the transformer is <3.5 dB over the 2.4-GHz ISM band, optimized to minimize the NF contribution. Besides, the transformer bandpass filtering response (see Fig. 8) leads to an effective harmonic suppression, with a simulated third-order harmonic rejection of 29 dB.

As depicted in [18, eq. (15)], the transformer insertion loss, switch ON-resistance ($R_{on,0}$) and also the harmonic-folding effect contribute to a sub-3-dB NF when the input-impedance matching (S_{11}) is <-15 dB. Here, our balun-LNA reveals a NF of 5 dB at 2.4 GHz. We believe that we can improve the NF by exploiting the silicon-on-insulator (SOI) technology that allows the realization of the transformer with a higher Q [11]. The NF is improved by 0.4 dB for a 30% enhanced Q in simulation. Besides, the implementation of the N-path SC filter with additional paths (e.g., $N = 8$) reduces the NF due to the harmonic-folding effect [19].

III. Pipeline Down-Mixing BB-Extraction Scheme

The I/Q BB signals $V_{BB,I0\pm}$ and $V_{BB,Q0\pm}$ already experience a passive RF-to-BB gain of $2(1 + A_v)$, with A_v upper-bounded by the layout constraints of the transformer. To surmount this limit originated by avoiding the use of g_m, we conceive a chain of passive-SC network [7] that can extract more gain from the N-path passive balun-LNA, as described below.

A. Concept of Pipeline Down-Mixing

Fig. 9 shows our pipeline down-mixing BB-extraction scheme under an anti-phase non-overlap LO. We notice a phenomenon in our daily life that we can fill a bucket with more water in a certain period by lining up the water taps, and then pass the water of the bucket mth to the next like a pipeline method. The water taps are alternate-controlled by LO_1 and LO_3, which is an anti-phase non-overlapping LO. When each water tap opens, its water fills the bucket together with the water injected from its front-adjacent bucket. At last, we will obtain more water owing to this pipeline method. Inspired by this, we propose a pipeline down-mixing BB-extraction scheme using a chain of passive-SC branches driven by the same set of LO as the balun-LNA.

B. Circuit Implementation and Simulation Results

To realize the aforesaid concept, each bucket corresponds to a capacitor, while the water taps are the switches driven by the same set of LO as the balun-LNA. Fig. 10 shows its circuit implementation with only one pipeline path. A_V with a paralleled SC network constitutes the passive balun-LNA, with A_V realized by a step-up triple-coil transformer (detailed in Section II). The following SC stages cross-connect alternately with the differential outputs ($V_{o,RF\pm}$) of the balun-LNA under an anti-phase non-overlap LO. The same pipeline method allows also the extraction of the differential and quadrature paths. As shown in Fig. 10, the frequency components at f_{LO}, $3f_{LO}, \ldots$ exist in the output of each pipeline stage, which will disappear at the differential outputs. The other frequency components at $2f_{LO}$, $4f_{LO}, \ldots$, are resulted from the harmonic-folding back terms, because the BB signals on the capacitors will be back up-converted during each LO cycle owing to the bidirectional transparency property of the switches.

Fig. 11 elucidates the pipeline down-mixing mechanism. We separate the pipeline down-mixing circuit in Fig. 10 into three pipeline down-mixing operations for $m = 0$, 1 and ≥ 2, respectively, to obtain dc voltage gain at the output of each pipeline stage. For simplicity, we connect to the circuit an antenna (not shown here) carrying a sinusoidal signal with a period $1/f_{LO}$, this input signal behaves akin to a square-shaped waveform at $V_{i,RF\pm}$ [20]. The signal at $V_{o,RF\pm}$ will be an anti-phase square shaped waveform with an amplification factor of A_V. When LO_1 is high, $V_{BB,I0+}$ equals $V_{o,RF-}$, and tracks $V_{i,RF+}$ via C_0 during the off-period of LO_1, which signifies that $V_{i,RF+}$ and $V_{o,RF-}$ are down-mixed to $V_{BB,I0+}$, performing a dc voltage gain of $1 + A_v$ at $V_{BB,I0+}$. Likewise, when LO_3 is high, $V_{BB,I0+}$ passes on to $V_{BB,I1+}$.

On the other hand, with $V_{i,RF+}$ and $V_{o,RF-}$ also down-mixed to $V_{BB,I1+}$, it leads to a dc voltage increment of $1 + A_v$ at $V_{BB,I1+}$. Thereby, the circuit reaches a $2(1 + A_v)$ dc voltage gain at $V_{BB,I1+}$ totally. Meanwhile, we have $V_{o,RF-}$ and $V_{o,RF+}$ down-mixed to $V_{BB,I2+}$ via C_2, with $V_{BB,I1+}$ passing on to $V_{BB,I2+}$ at LO_1, and so on for the mth pipeline stage. There will be always a $2A_v$ dc voltage increment for every pipeline stage for $m \geq 2$, with $V_{o,RF+}$ and $V_{o,RF-}$ alternate-stacked on its front-adjacent stage output (i.e., $V_{BB,(m-1)+}$).

As such we can progressively extract and stack the gain from the balun-LNA using additional pipeline stages. Finally, we can obtain a differential dc voltage gain of $2[2(1 + A_v) + 2(M - 1)A_v]$ at the Mth pipeline stage, illustrated by (10), as shown at the bottom of the next page. For instance, in Fig. 12(a) a theoretical M of 263 can yield a 70-dB gain. Herein, we choose $M = 9$ to generate a 40.9-dB gain from the entire passive RF front-end at no load condition. Such a large

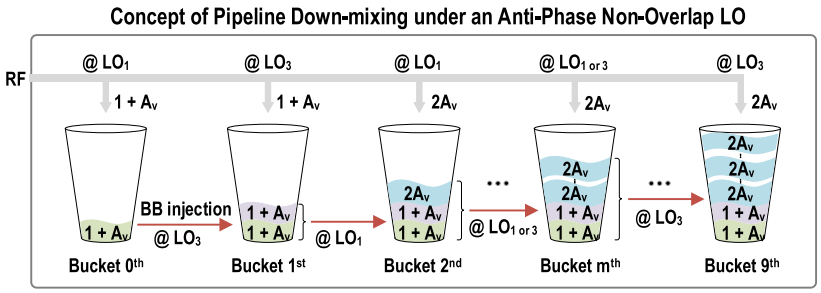

Fig. 9. Concept of the pipeline down-mixing BB-extraction scheme under an anti-phase non-overlap LO.

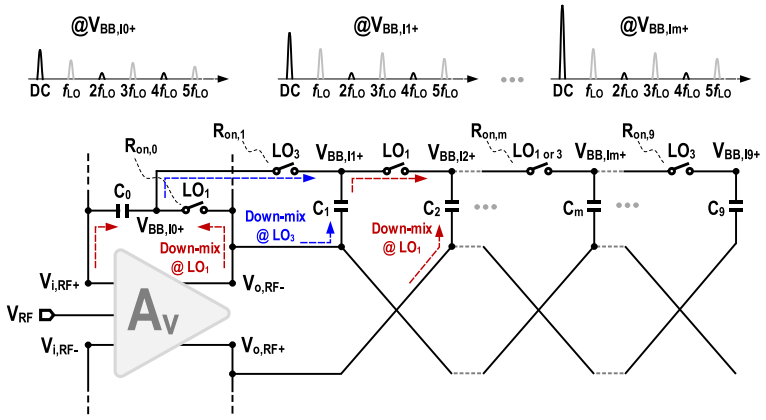

Fig. 10. Circuit implementation of the proposed pipeline down-mixing BB-extraction scheme with only one pipeline path shown. The quadrature and differential path are similar.

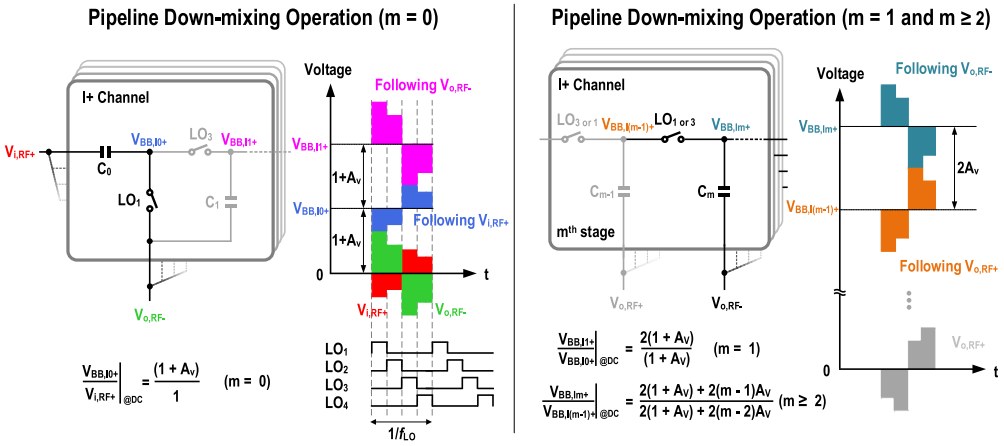

Fig. 11. Explanation of the pipeline down-mixing BB-extraction operation. Assuming an ideal passive voltage gain and the switches modeled as ideal with a series resistance.

gain effectively lowers the noise contribution of the subsequent BB circuitry, as well as its power budget. The initial gain increment is alike the Fibonacci sequence [see Fig. 12(a)], and grows slower than the Fibonacci sequence due to the constant voltage increment (i.e., $2A_V$), whereas the Fibonacci sequence shows a ~1/0.618 (i.e., 4 dB) gain increment for each stage.

C. Design Considerations

Although the dc voltage increases continuously with the pipeline numbers, each pipeline capacitor (C_{1-M}) can create a charge sharing effect, narrowing down the signal BW. The equivalent capacitance due to charge sharing is $4C_1$ created

$$H_M(j\omega_{in}, j\omega_{out})|_{@\omega_{out}=0} = \left.\frac{V_{BB,IM+} - V_{BB,IM-}}{V_{i,RF+}}\right|_{@\omega_{out}=0}$$
$$= 2(1+A_V)\cdot\frac{2(1+A_V)}{1+A_V}\cdot\frac{2(1+A_V)+2A_V}{2(1+A_V)}\cdots\frac{2(1+A_V)+2(m-1)A_V}{2(1+A_V)+2(m-2)A_V}\cdots\frac{2(1+A_V)+2(M-1)A_V}{2(1+A_V)+2(M-2)A_V} \quad (10)$$

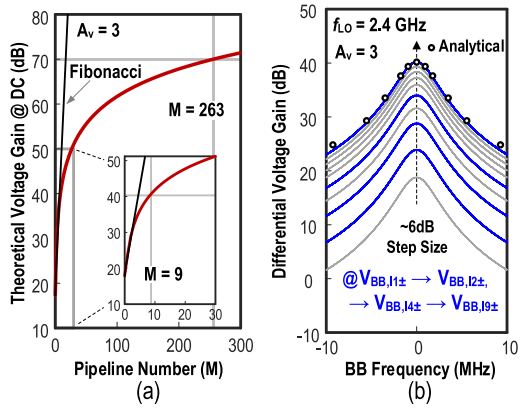

Fig. 12. (a) Theoretical voltage gain versus the pipeline number. (b) Simulated differential voltage gain response at each pipeline stage output. The four-step gain control is with a ~6-dB step size.

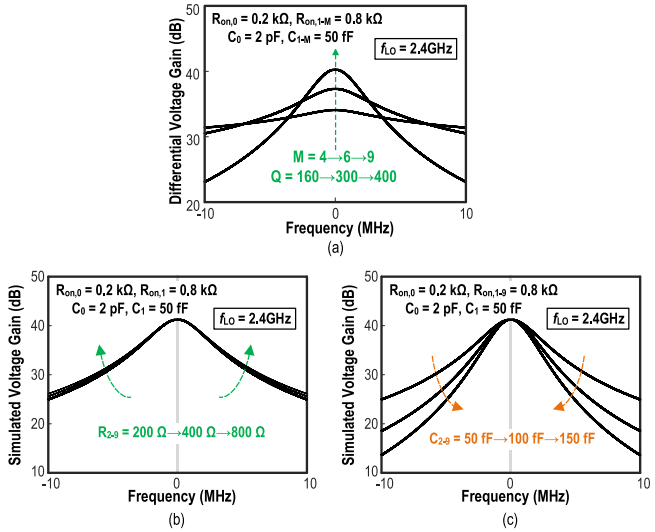

Fig. 13. (a) BW narrowing effect due to the charge sharing of each pipeline capacitor. (b) Simulated gain response against the pipeline switch ON-resistance. (c) BW scales down as the pipeline capacitance increases.

by the passive Miller effect between $V_{\mathrm{BB},I0+}$ and $V_{\mathrm{BB},I1+}$ (i.e., $2\times$ passive voltage gain) for the first pipeline stage ($m = 1$). Similarly, each C_m will share the charge with its front-adjacent pipeline capacitor (C_{m-1}) by creating an equivalent capacitance of $\{[2(1 + A_{\mathrm{V}}) + 2(m - 1)A_{\mathrm{V}}]/[2(1 + A_{\mathrm{V}}) + 2(m - 2)A_{\mathrm{V}}]\}^2 C_m$ ($m \geq 2$). After the iteration, the total equivalent capacitance sharing charge with C_0 becomes

$$C_{\mathrm{eq}} = \left[\frac{2(1+A_{\mathrm{V}})}{1+A_{\mathrm{V}}}\right]^2 \cdot \left\{C_1 + 0.5 \cdot \frac{2(1+A_{\mathrm{V}}) + 2A_{\mathrm{V}}{}^2}{2(1+A_{\mathrm{V}})} \cdot \left\{C_2 + \cdots + 0.5 \cdot \left[\frac{2(1+A_{\mathrm{V}}) + 2(m-1)A_{\mathrm{V}}}{2(1+A_{\mathrm{V}}) + 2(m-2)A_{\mathrm{V}}}\right]^2 \cdot \left\{C_m + \cdots + 0.5 \cdot \left[\frac{2(1+A_{\mathrm{V}}) + 2(M-1)A_{\mathrm{V}}}{2(1+A_{\mathrm{V}}) + 2(M-2)A_{\mathrm{V}}}\right]^2 C_{\mathrm{M}}\right\}\right\}\right\}. \tag{11}$$

The factor 0.5 emerges from the cross-connected structure between $V_{\mathrm{o,RF+}}$ and $V_{\mathrm{o,RF-}}$ like the differential mode. On the other hand, $R_{\mathrm{on},1}$ can affect the input impedance by means of parallelizing with $R_{\mathrm{on},0}$. To address this we design $R_{\mathrm{on},1}$ with 0.8 kΩ that is $4\times$ larger than $R_{\mathrm{on},0}$. Taking the effect of C_{eq} and $R_{\mathrm{on},1}$ into consideration, we can roughly obtain the RF-to-BB gain response at the output of Mth pipeline stage as

$$H_M(\mathrm{j}\omega_{\mathrm{in}}, \mathrm{j}\omega_{\mathrm{out}}) = \frac{H_M(\mathrm{j}\omega_{\mathrm{in}}, \mathrm{j}\omega_{\mathrm{out}})|_{@\omega_{\mathrm{out}}=0} \cdot \mathrm{sinc}(\pi/N \cdot \omega_{\mathrm{in}}/\omega_{\mathrm{LO}})}{1 + \mathrm{j}\omega_{\mathrm{out}} 2\left(R_{\mathrm{S}} + \frac{R_{\mathrm{on},0}||R_{\mathrm{on},1}}{1+T+2k_{23}\sqrt{T}}\right)(1+T+2k_{23}\sqrt{T})(C_0+4C_{\mathrm{eq}})}. \tag{12}$$

Considering the charge sharing effect, herein, we choose nine pipeline stages, which can generate a 40.9-dB gain to lower the BB noise contribution and its power budget effectively. Fig. 12(b) shows the simulated differential voltage gain at each pipeline stage output. As illustrated in (12), once we choose the pipeline number, the selectivity is the same at each pipeline stage output, except the voltage gain difference. By bypassing partial pipeline stages and extracting the voltage from the selected outputs: $V_{\mathrm{BB},I1\pm}$, $V_{\mathrm{BB},I2\pm}$, $V_{\mathrm{BB},I4\pm}$, and $V_{\mathrm{BB},I9\pm}$, we can pull out the gain by a four-step gain control with ~6-dB step size. In Fig. 12(b), we plot (12) at 2.4 GHz, which matches well with the simulated result in the RF frequency range from 2.39 to 2.41 GHz. From (11), C_{eq} is 1.62 pF for the given parameters $A_{\mathrm{V}} = 3$ and $C_{1-9} = 50$ fF. Simulated at 2.4 GHz [see Fig. 13(a)], the Q factor increases from 160 to 400 as the pipeline number (M) goes from 4 to 9. Since LO_1 and LO_3 are anti-phase with each other, the switch ON-resistance from $R_{\mathrm{on},2}$ to $R_{\mathrm{on},9}$ (see Fig. 10) does not affect the RF input impedance. Fig. 13(b) shows that the switch ON-resistance ($R_{\mathrm{on},2-9}$) can hardly affect the gain response in simulation. Yet, the pipeline switch size plays a key role on the power consumption. A small switch size (0.3 μm/30 nm, $R_{\mathrm{on},2-9} = 0.8$ kΩ) with tiny parasitic allows low dynamic power consumption of the LO buffers. Considering that the large RC time constant of the passive-SC network can narrow the signal BW [see Fig. 13(c)], a small C_{1-9} (50 fF) aids to uphold a BB BW of ~3 MHz. The phase noise from LO will accumulate through the nine pipeline stages, and degrades the receiver NF by 0.6 dB (simulation) when an LO source with a phase noise of -120 dBc/Hz at 1 MHz offset is employed.

IV. Hybrid Complex Filter

Fig. 14 displays the BB hybrid complex filter, which provides the functions of BB gain, image rejection and channel selection. A high-order RC-CR polyphase filter allows a more robust image rejection without degrading the linearity when compared with its active counterpart. Yet, it narrows the BW significantly when connected to the passive RF front-end due to the limited drive capability of the passive RF front-end. To address this, we apply a G_m-C complex filter in the first stage. Similar to [21], we model its principle as presented in Fig. 15(a). Aided by $C_{\mathrm{B1,2}}$, we create a complex-pole input

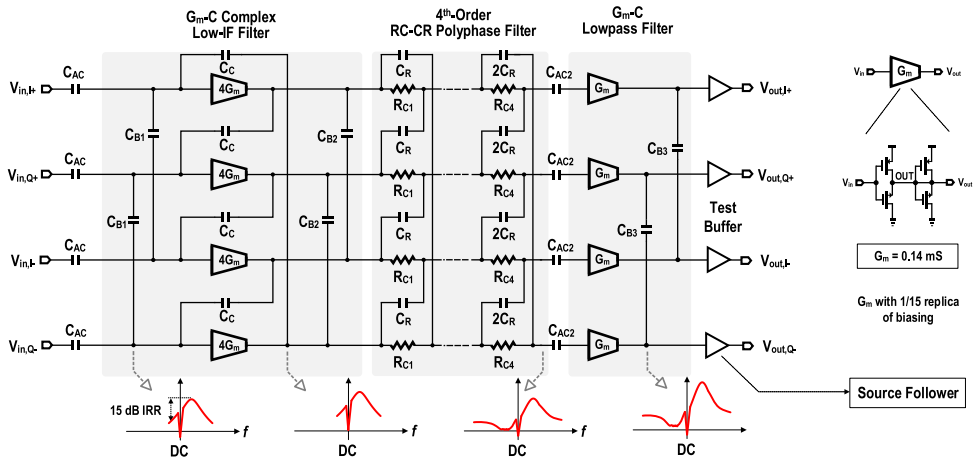

Fig. 14. Low-IF hybrid complex filter.

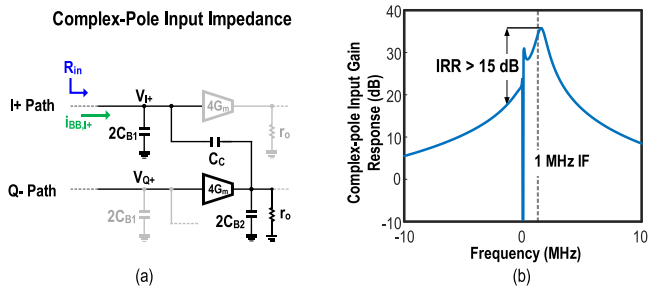

Fig. 15. (a) Complex-pole input impedance analysis and (b) simulated IRR of >15 dB achieved at the input of the hybrid complex filter.

impedance at the input of the forefront G_m-C complex low-IF filter, defined as below

$$R_{\text{in,BB}} = \frac{1}{s}\cdot\frac{s\cdot(C_{\text{C}}+2C_{\text{B2}})/(C_{\text{C}}+2C_{\text{B1}})+r_{\text{O}}/(C_{\text{C}}+2C_{\text{B1}})}{s\cdot[2C_{\text{B2}}+C_{\text{C}}||(2C_{\text{B1}})]+\text{j}4G_{\text{m}}C_{\text{C}}/(C_{\text{C}}+2C_{\text{B1}})+1/r_{\text{O}}} \tag{13}$$

with the complex pole located in

$$s_{\text{P}} = -\frac{1}{r_{\text{O}}\cdot[2C_{\text{B2}}+C_{\text{C}}||(2C_{\text{B1}})]}+\frac{\text{j}4G_m}{2C_{\text{B1}}+2C_{\text{B2}}(1+2C_{\text{B1}}/C_{\text{C}})}. \tag{14}$$

The real part derives from the output impedance (r_{O}) of the $4G_m$ stage, whereas the I/Q-cross-connected $4G_m$ stages determine the imaginary part. The complex-pole input impedance offers a simulated IRR of >15 dB before the amplification of the image by the $4G_m$ stages. Fig. 15(b) plots the simulated gain response with the low-IF at +1 MHz. C_{B2} also benefits the OOB rejection at the output of the $4G_m$ stages by creating a real pole located in $-1/[r_{\text{O}}(2C_{\text{B2}}+C_{\text{C}})]$. The G_m-C complex filter is ac-coupled with the passive RF front-end. A large dc blocking capacitor (C_{AC}) can reduce the voltage gain loss given by $C_{\text{AC}}/(C_{\text{AC}}+2C_{\text{B1}})$, but at the cost of chip area. With an affordable C_{AC} (10.5 pF), C_{B1} = 1.3 pF yields an acceptable gain loss of 1.9 dB.

The middle stage is a fourth-order *RC-CR* polyphase filter to deepen and widen the IRR coverage over the image band (−1.5 to −0.5 MHz) which can meet the required IRR robustly (21 dB for BLE standard). The passive *RC-CR* network causes a 7.3 dB voltage gain loss in simulation. To suppress the near-band images at −0.5 MHz, we design the fourth stage as 175 kΩ and 1.8 pF, with the other three stages designed as 0.9 pF, with 115, 150 and 175 kΩ, respectively. The final ac-coupled G_m-C lowpass filter offers more BB gain and OB rejection, and drives the test buffers. We design the tranconductor (i.e., G_m) as a 4× scaled replica of $4G_m$. Another dc blocking capacitor (C_{AC2}) with 1 pF results in a 0.8-dB voltage gain loss according to the simulation. The passive RF front-end loaded with the BB hybrid filter shows a simulated gain drop from 40.9 to 36 dB. Due to the high-voltage gain (i.e., 36 dB) provided by the passive RF front-end, each $4G_m$ is 0.56 mS, only consuming a 15-μA dc current. All $4G_m$ and G_m stages are inverter-based amplifiers due to their high current-to-g_{m} efficiency as in [8]. Each amplifier is biased by a 1/15th scaled replica of its circuit with the input and output shorted. The hybrid filter shows a simulated voltage gain of 25 dB.

V. Four-Phase 25%-Duty-Cycle LO Generator

Fig. 16 displays the non-overlap 25%-duty-cycle LO generator [22]. We apply the 50-Ω matching resistors at the input to obtain compliance with the external signal generator, and the input clock signals ($\text{CLK}_{\text{IN,P}}$, $\text{CLK}_{\text{IN,N}}$) ac-coupled to the input buffer. Resistive-feedback input buffers amplify $\text{CLK}_{\text{IN,P}}$ and $\text{CLK}_{\text{IN,N}}$ that operate at $2f_{\text{LO}}$. After the adjustment by a phase corrector, a div-by-2 circuit which is composed of two differential latches clocked by opposite phases of $2\text{LO}_{\text{P,N}}$ generates the four-phase 50%-duty-cycle signals $Q_{1,2}$ and $\overline{Q_{1,2}}$ (operating at f_{LO}). By performing an "AND" operation on $2\text{LO}_{\text{P,N}}$ and $Q_{1,2}$ and $\overline{Q_{1,2}}$, we can generate the four-phase 25%-duty-cycle LO waveforms (LO_{1-4}). To save the dynamic power, we utilize low-threshold transistors. Powered at a 0.6-V supply, the LO generator consumes 191 μW at 2.4 GHz, with 144 μW from the switch buffer. The mismatch of four-phase 25%-duty-cycle LO is analyzed similar to [17], a 10% of LO duty cycle error will induce a variation of IB voltage gain by 0.2 dB and maintains passband center frequency unchanged,

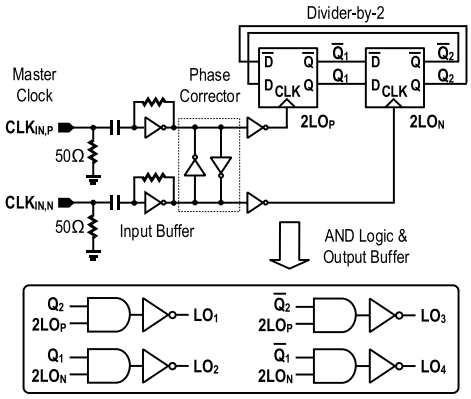

Fig. 16. Four-phase 25%-duty-cycle LO generator.

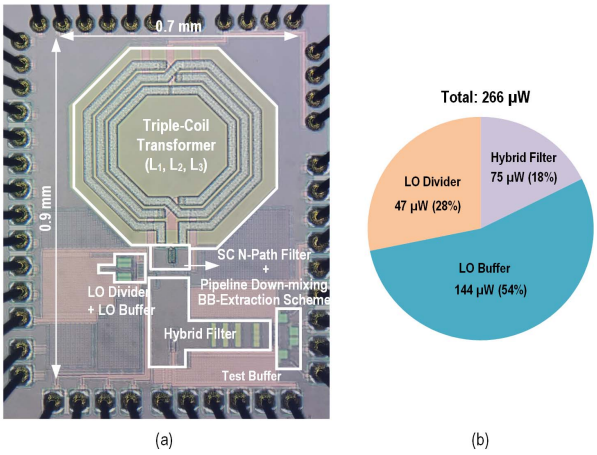

Fig. 17. (a) Chip micrograph and (b) power consumption of the BLE receiver prototyped in 28-nm CMOS.

while a 5° phase error only results in a 0.1-dB variation of IB voltage gain in simulation. We extract the load of the LO generator, which is ~34.4 fF for each 25%-duty-cycle LO path by the elaborately layout design. In the post-layout simulation, the LO generator exhibits a phase noise of −149.1 dBc/Hz at an 80-MHz offset.

VI. Measurement Results

Fig. 17(a) presents the chip photograph of our BLE receiver fabricated in TSMC 28-nm CMOS. The active area is 0.5 mm^2 dominated by the transformer. We use two external Baluns (Mini-Circuits ADT4-6T+) at the four-phase BB outputs to interface with the single-ended equipment. The loss due to the PCB trace and cable is de-embedded. Fig. 17(b) illustrates the power consumption breakdown of the BLE receiver. The total power consumption is 266 μW, with 75 μW from the hybrid complex filter at a 1-V supply. The LO divider and LO buffer at 0.6-V supply contribute with the remainder. Without g_m, the passive-intensive RF front-end does not consume static power.

Our chip is packaged with the chip-on-board (COB) method and measured under a PCB assembly, in which the inductance effect of the bondwire should be considered. In simulation, we model the bondwire as a 1 nH series inductor and a 0.1-pF shunt capacitor, which match well with the measurements.

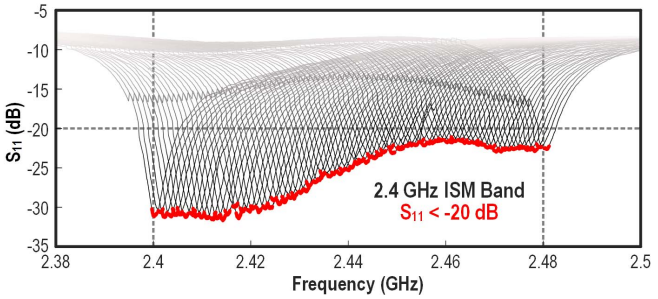

Fig. 18. Measured S_{11} over the 2.4-GHz ISM band.

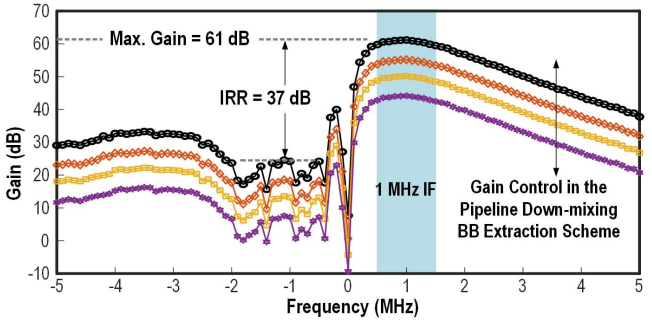

Fig. 19. Measured RF-to-BB gain response with a four-step gain control.

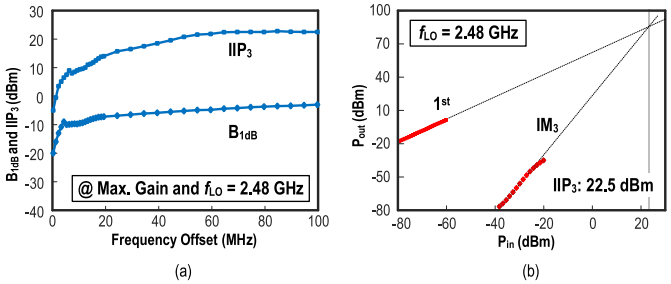

Fig. 20. Measured (a) IIP_3 and $B_{-1\,dB}$ profiles of the BLE receiver and (b) OOB-IIP_3 profile at 80 MHz offset.

Fig. 18 shows the measured S_{11}, which is <-20 dB in the channel level that aligns with the LO frequency over the entire 2.4-GHz ISM band. Fig. 19 plots the RF-to-BB gain response, in which the maximum RF-to-BB gain is 61 dB at 1-MHz IF, and the measured IRR is 37 dB due to the complex-pole input impedance and the fourth-order *RC-CR* polyphase filter. The simulated worst gain variation at a 1-MHz IF is 1.3 dB from 100× Monte-Carlo simulations. We also measured ten chip samples and the gain variation is <0.5 dB, which matches well with the simulated results. The deviation of IRR from simulations is mainly caused by process mismatch, which can be improved further by symmetrical layout techniques. By controlling the pipeline numbers in the *pipeline down-mixing BB-extraction scheme*, the voltage gain varies from 44 to 61 dB with ~6-dB step size.

Fig. 20 shows the receiver linearity assessed by IIP_3 and $B_{-1\,dB}$.The measured OOB-IIP_3 and OOB-$B_{-1\,dB}$ are 22.5 and −3 dBm at 80 MHz offset, respectively. A two-tone test at $[f_{LO} + \Delta f]$ and $[f_{LO} + 2\Delta f - (IF + 0.1\ MHz)]$ perform the IIP_3 profile. Fig. 21(a) displays the measured NF over the desired ISM band at different gain steps. Measured

TABLE I
PERFORMANCE SUMMARY AND BENCHMARK WITH THE STATE-OF-THE-ART

	This Work	JSSC'21 [8]	ISSCC'17 [2]	ISSCC'15 [3]	JSSC'22 [33]
Applications	BLE	BLE / BT5.0 / IEEE 802.15.4	BLE	BLE	BLE
IF	Low-IF	Zero-IF	Zero-IF	Low-IF	Low-IF
RF Gain Stage	**Passive** Balun-LNA + SC N-Path Filter	**Active** Push-Pull LNA	**Active** Ultra-Low-Voltage Two-Stage LNA	**Active** Quadrature LNA	**Active** Unbalanced Gain-Boosted LNA
1st BB Gain Stage	**Passive** Pipeline Down-Mixing BB Extraction	**Active** Transimpedance Amplifier	**Active** Voltage Amplifier	**Active** Transimpedance Amplifier	**Active** Voltage Amplifier
Active BB Filter	5 Complex Poles + 2 Real Poles	2 Real Poles + Analog FIR	3 Real Poles	2 Complex Poles	2 Complex Poles
External Components	No	No	No	Yes	No
Supply Voltage (V)	0.6 & 1.0	0.7	0.18	0.8	1
Analog Power (μW)	75	329	230	476	250
LO Divider + Buffer Power (μW)	191	41	N/A	N/A	150
Total Power (μW)	266	370	230 (VCO Excluded)	476 (VCO Excluded)	400
Maximum Gain (dB)	61	61	34.5	56.1	50
NF (dB)	6.1	5.5	11.3	15.8	6.8
OOB-B_{-1dB} (dBm)	**-3**	**-22**	**-27.5**	**N/A**	**-16**
OOB-IIP_3 (dBm)	**22.5**	**-7.5**	**-12.5**	**-16.8**	**-0.35**
SFDR (dB) @ SNR_{min}=10dB	**77**	**57.3**	**50.1**	**44.3**	**61.5**
IRR (dB)	37	N/A	N/A	37.3	26.4
Active Area (mm^2)	0.5	0.5	1.35 (VCO Excluded)	0.25	0.175
Technology	28 nm CMOS	22 nm FDSOI	28 nm CMOS	130 nm CMOS	28 nm CMOS

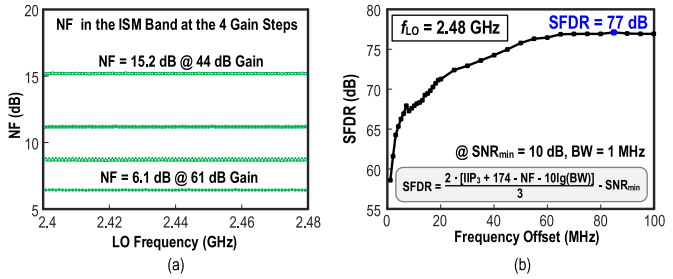

Fig. 21. Measured (a) NF at different gain steps and (b) SFDR at a SNR_{min} = 10 dB for different frequency offsets.

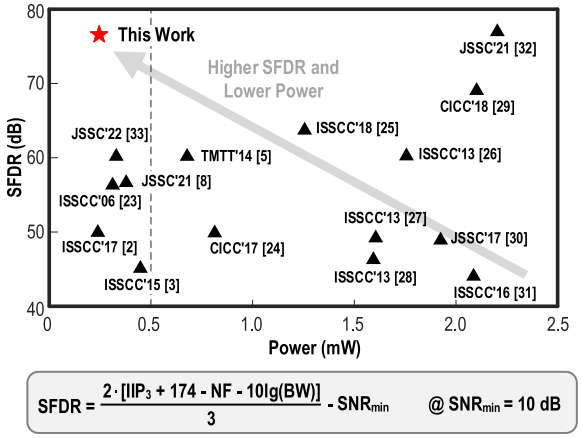

Fig. 22. Benchmark with the state-of-the-art BLE receivers in terms of SFDR and power consumption.

at 61-dB gain, the NF is 6.1 dB, and up to 15.2 dB at 44-dB gain with the partial pipeline stages bypassed. The NF is insensitive to the blocker power level, which only degrades 0.25 dB when the injected blocker power is −30 dBm at an 80-MHz offset. Measured at the maximum gain (61 dB), the NF degrades to 15 dB when the blocker power is −10 dBm. From simulation, the phase noise of the LO is −145.5 dBc/Hz at 2.5 MHz offset, which is ∼10 dB worse than [8], and both are well beyond the requirement of the BLE standard according to [2]. In Fig. 21(b), we show the measured SFDR under a 10-dB SNR_{min} and 1-MHz BW for different frequency offsets. Measured at 2.48 GHz, the OOB-SFDR is 77 dB and IB-SFDR is >58 dB. Fig. 22 illustrates the SFDR against power benchmark with state-of-the-art BLE receivers [5], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32]. Thanks to the passive RF front-end, the proposed receiver achieved the best-in-class SFDR of 77 dB at <0.5 mW power budget. The measured LO leakage at the RF port is −61 dBm at 2.4 GHz, due to the weak isolation between the LO and RF ports. Similar to the *N*-path filter-based techniques [9], [10], [11], [12], our receiver also faces harmonic folding, especially the third- and fifth-order terms. The measured third-order and fifth-order harmonic-folding rejection ratio ($HFRR_3$ and $HFRR_5$) are 31.3 and 27 dB, respectively, which are ascribed to the lowpass filtering of our transformer that provides prefiltering of these folding terms.

Table I summarizes the key performance of the BLE receiver and benchmarks it with the state-of-the-art. Comparing to

the recent ULP BLE receivers with active RF front-ends, our receiver features a passive balun-LNA + SC N-path filter in the RF gain stage, and a passive pipeline down-mixing BB-extraction scheme in the first BB stage. Without g_m nonlinearity, they jointly offer a high-Q bandpass characteristic to suppress the OOB blockers while generating a large voltage gain to suppress the noise contribution of the BB circuitry, concurrently improving the NF and OOB-IIP$_3$. When compared with [8], the power budget, NF, and area budget are comparable; however, our receiver delivers $\sim$20 dB better SFDR and 19 dB better OOB-B$_{-1\,dB}$. This work achieves comparable power budget with respect to [2], and consumes 44.1% less power than [3] and 33.5% less power than [33]. We deduce the VCO power consumption from [2] and [3]. At sub-0.5-mW power budget, the improved NF and OOB-IIP$_3$ together result in the best-in-class SFDR (77 dB) and OOB-B$_{-1\,dB}$ (-3 dBm) without burdening the power budget (266 μW).

VII. Conclusion

We reported an N-path passive balun-LNA and a pipeline down-mixing BB-extraction scheme to improve the SFDR of a BLE receiver at low power. The former, involving no g_m, performed voltage amplification along with high-Q bandpass filtering and input-impedance matching. The latter, also with no g_m, realized passively the first-BB gain stage, suppressing the noise contribution of the remaining BB circuitry. The only dynamic power is from the LO generator. The final stage is a low-power hybrid complex filter offering an additional gain and a complex-pole input impedance to enhance the IRR. Fabricated in TSMC 28-nm CMOS, the proposed BLE receiver scored a 6.1-dB NF and a 22.5-dBm OOB-IIP$_3$ at a 61 dB maximum gain, while consuming only 266 μW. The corresponding SFDR is 77 dB and OOB-B$_{-1\,dB}$ is -3 dBm.

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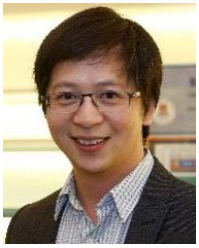

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